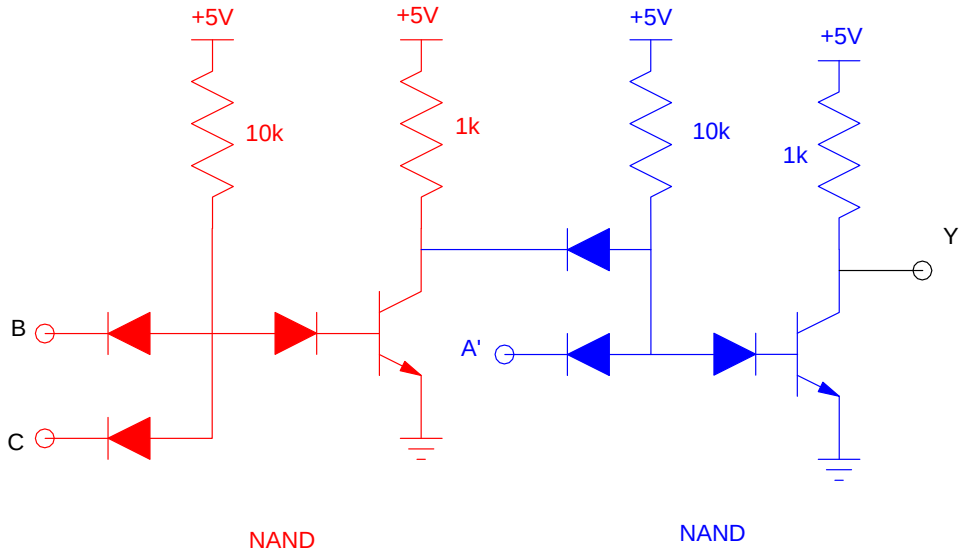
ECE 320 - Homework #7

DTL, TTL Logic. Due Monday, October 12th

1) The following circuit implements Y = f(A, B, C) using DTL NAND gates:

Assume $\beta = 100$



1) What function does this implement?

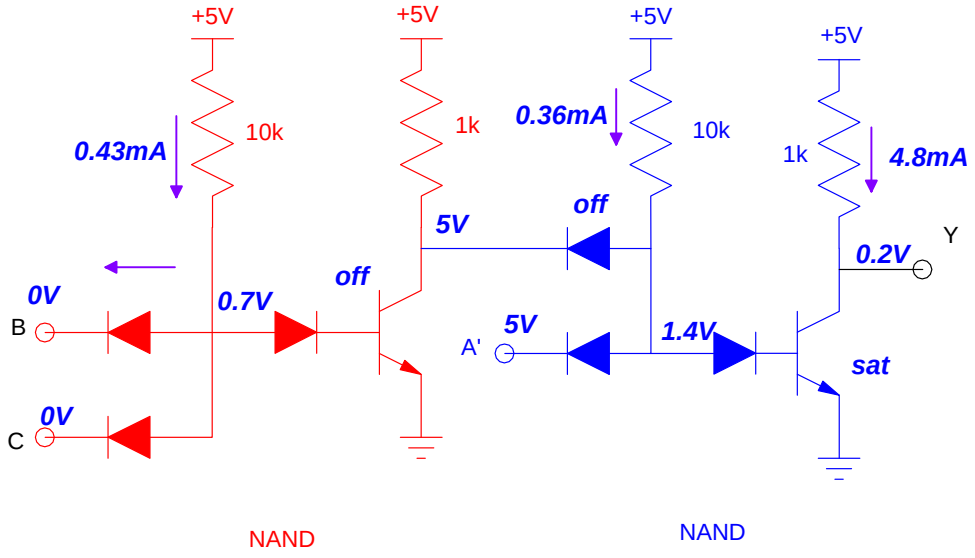
$$Y = \overline{\left(\left(\overline{BC}\right)\overline{A}\right)}$$

$$Y = \overline{\left(\overline{BC}\right)} + A$$

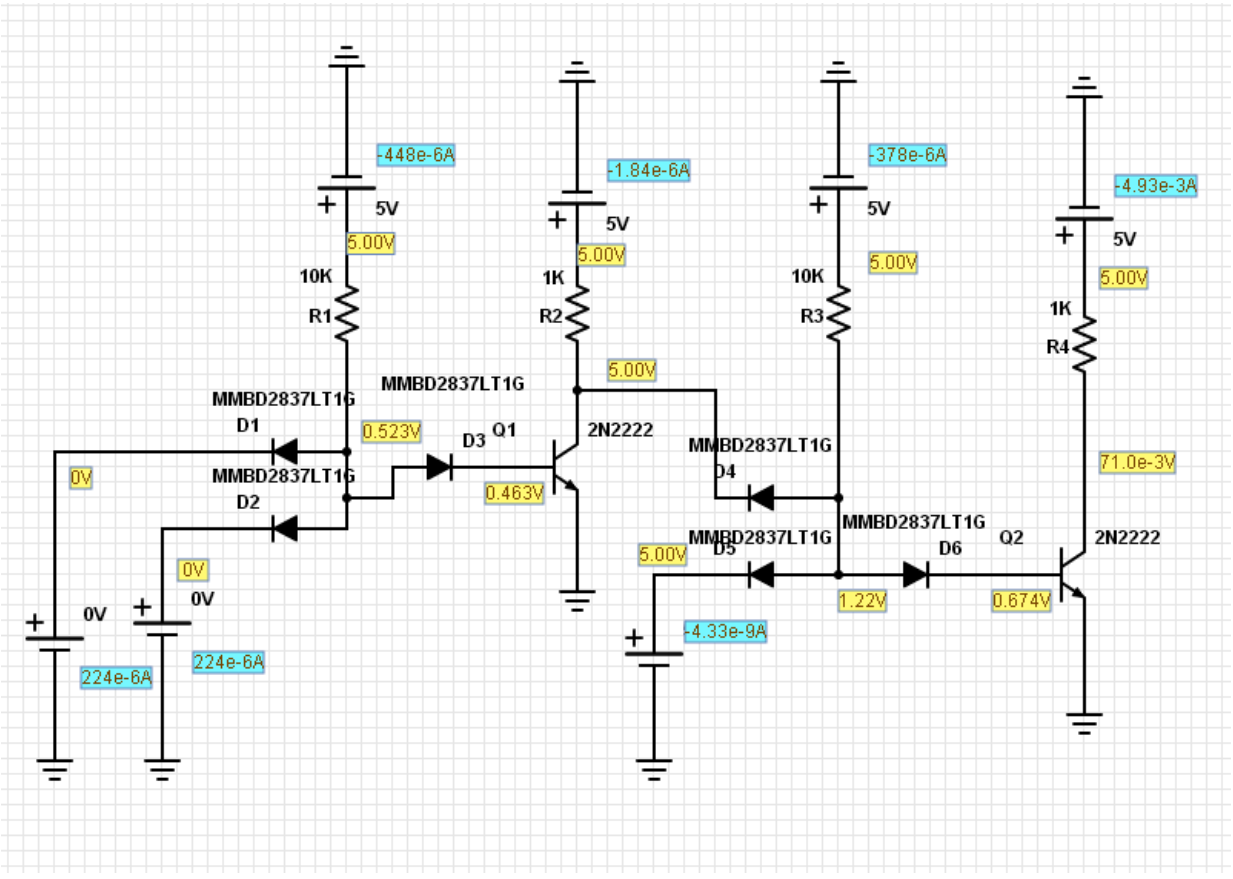
$$Y = A + BC$$

2) Determine the voltages and currents for

A = B = C = 0V.

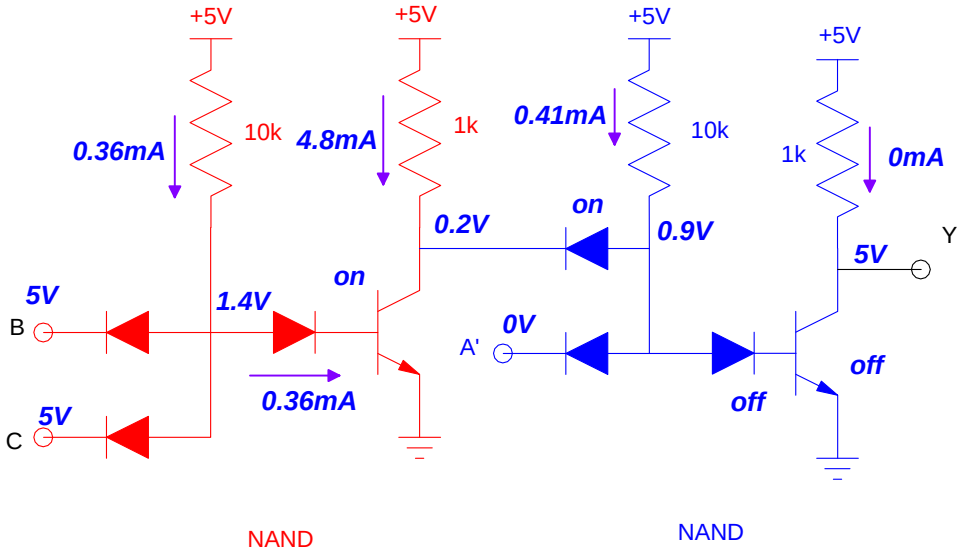


4) Check with PartSim

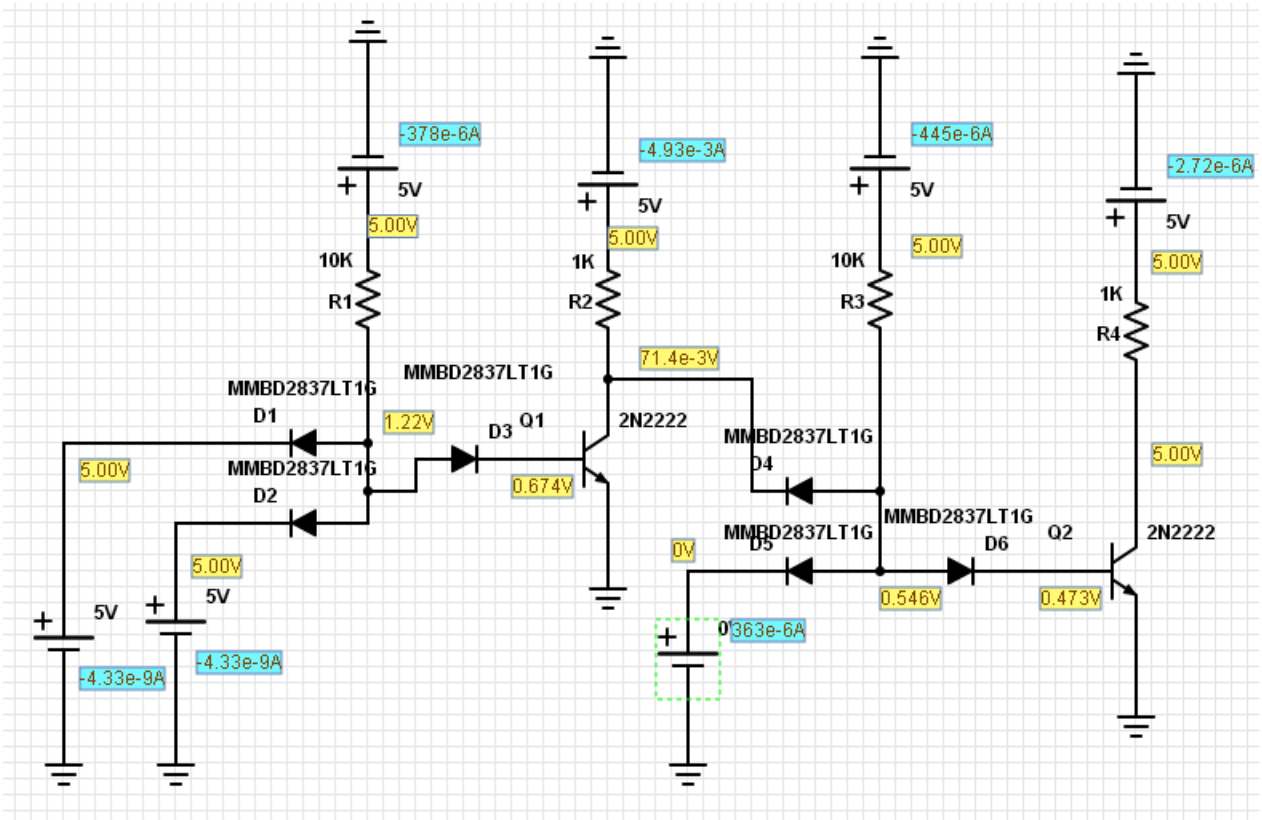


3) Determine the voltages and currents for

A = B = C = 5V



4) Check your results in PartSim.

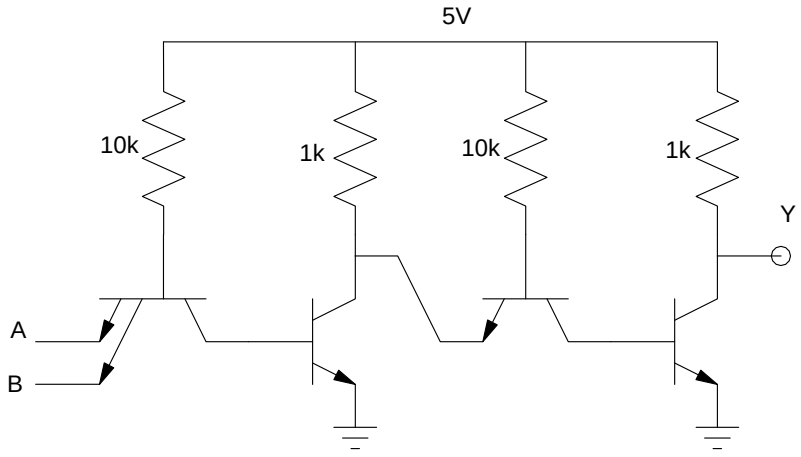


5) The following circuit implements a function using TTL logic

Will be due next week

Assume

- $\beta = 100$ (NPN used correctly)
- $\beta = 0.1$ (NPN used in reverse)



5) What is the logic for this circuit?

6) Determine the voltages and currents for

A = B = 5V

7) Determine the voltages and currents for

A = B = 0V

Lab: (term project)

Combine two or more of the circuits we've covered this semester into one project.

8) Requirements: Specify what your circuit is going to do

- Inputs
- Outputs
- Relationship

9) Project Breakdown: Show how your project splits into two (or more) sections - each being a circuit we covered in ECE 320

10) Requirements for each section: For each sub-circuit, specify its

- Inputs
- Outputs
- Relationship

Lab for the rest of ECE 320: for each section

- Analysis: Paper design (including calculations) for a circuit which satisfies it's design requirements
- Test: Simulation in PartSim to check your calculations
- Validation: Build that section in lab, collect data to show it does actually meet its requirements.