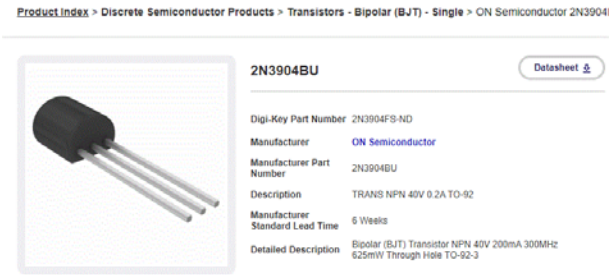
ECE 320 - Homework #8

Boolean Logic, DTL, TTL Logic. Due Monday, October 21st

Transistor Data Sheets

1) Find the data sheets for a 3904 transistor. From the data sheets, determine



V_{be} @ 20mA

- Ib = 1mA: 0.65V < Vbe < 0.85V
- Ib = 5mA Vbe < 0.95V

$V_{ce(sat)}$

- Ic = 10mA Vce < 0.2V
- Ic = 50mA Vce < 0.3V

$h_{FE} = \beta$

- Ic = 0.1mA hFE > 40
- Ic = 1mA hFE > 70
- Ic = 10mA 100 < hFE < 300
- Ic = 50mA hFE > 60
- Ic = 100mA hFE > 30

$I_{c(max)}$

- 200mA

Absolute Maximum Ratings(1), (2)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Value	Unit
V_{CEO}	Collector-Emitter Voltage	40	V
V_{CBO}	Collector-Base Voltage	60	V
V_{EBO}	Emitter-Base Voltage	6.0	V
I_C	Collector Current - Continuous	200	mA
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C

ON CHARACTERISTICS(5)					
h_{FE}	DC Current Gain	I_C = 0.1 mA, V_{CE} = 1.0 V	40		
		I_C = 1.0 mA, V_{CE} = 1.0 V	70		
		I_C = 10 mA, V_{CE} = 1.0 V	100	300	
		I_C = 50 mA, V_{CE} = 1.0 V	60		
		I_C =100 mA, V_{CE} = 1.0V	30		
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA		0.2	V
		I_C = 50 mA, I_B = 5.0 mA		0.3	
V_{BE}(sat)	Base-Emitter Saturation Voltage	I_C = 10 mA, I_B = 1.0 mA	0.65	0.85	V
		I_C = 50 mA, I_B = 5.0 mA		0.95	

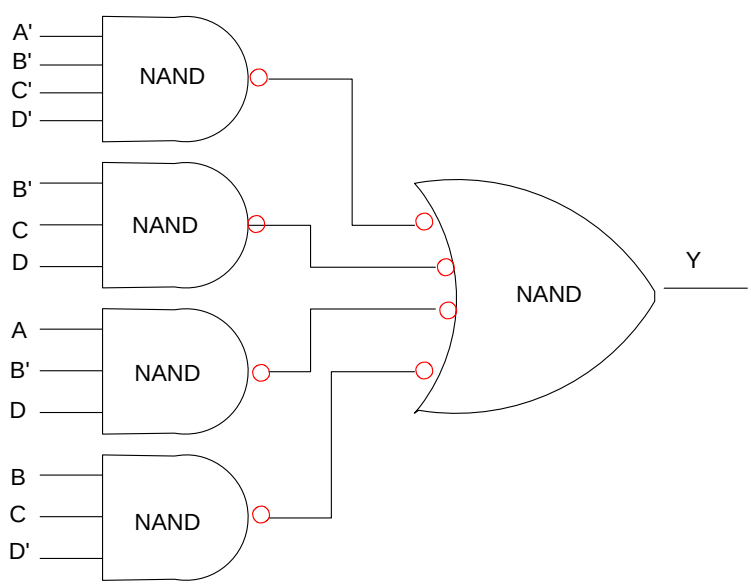
Boolean Logic

2) Design a circuit using NAND gates to implement Y(A,B,C,D) (i.e. circle the 1's)

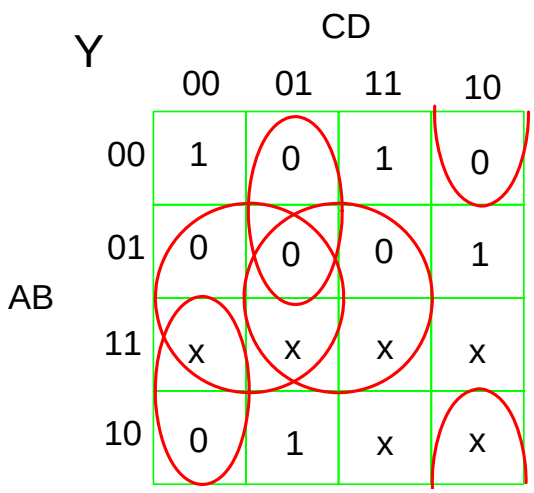
Y	CD 00	CD 01	CD 11	CD 10
AB 00	1	0	1	0
AB 01	0	0	0	1
AB 11	x	x	x	x
AB 10	0	1	x	x

This gives

$$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{B}CD + A\overline{B}D + BC\overline{D}$$



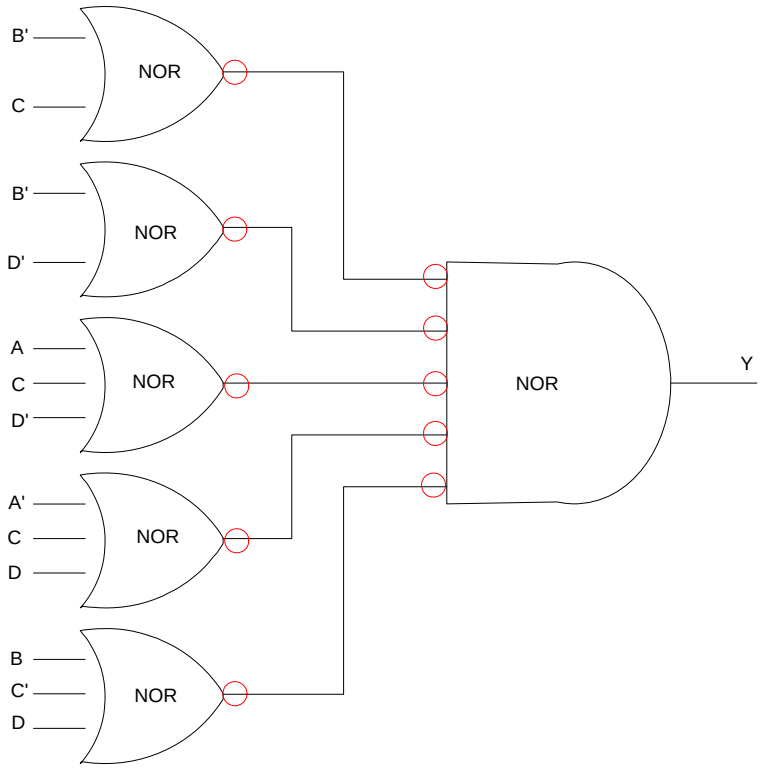
3) Design a circuit using NOR gates to implement Y(A,B,C,D) (i.e. circle the 0's)



$$\overline{Y} = B\overline{C} + BD + \overline{A}\overline{C}D + A\overline{C}\overline{D} + \overline{B}C\overline{D}$$

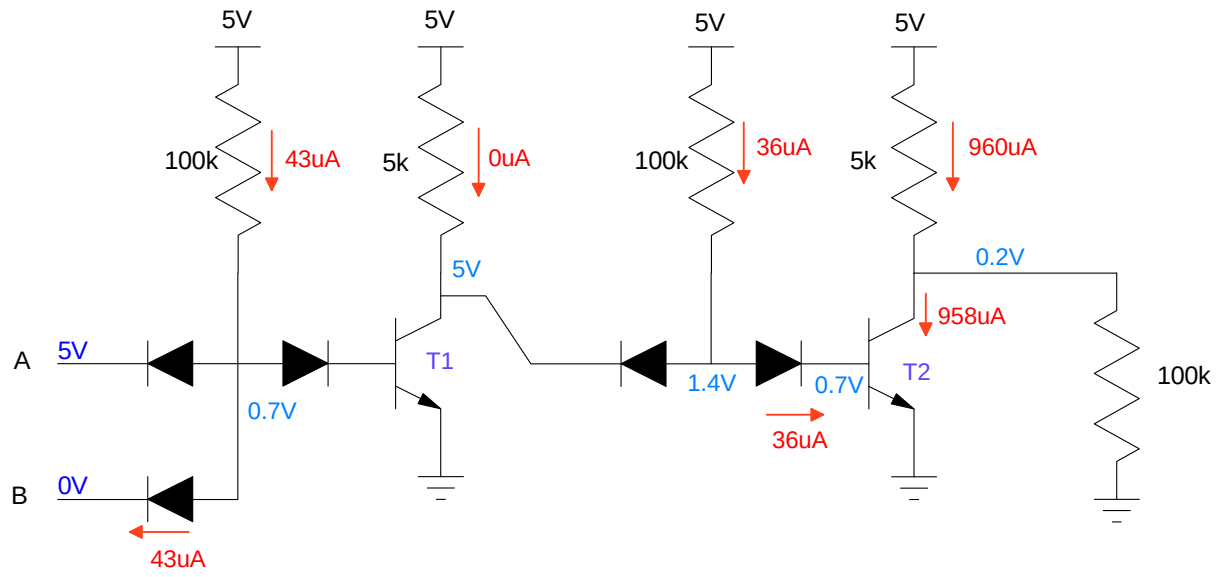
Use DeMorgan's theorem

$$Y = \left(\overline{B} + C\right)\left(\overline{B} + \overline{D}\right)\left(A + C + \overline{D}\right)\left(\overline{A} + C + D\right)\left(B + \overline{C} + D\right)$$



DTL Logic

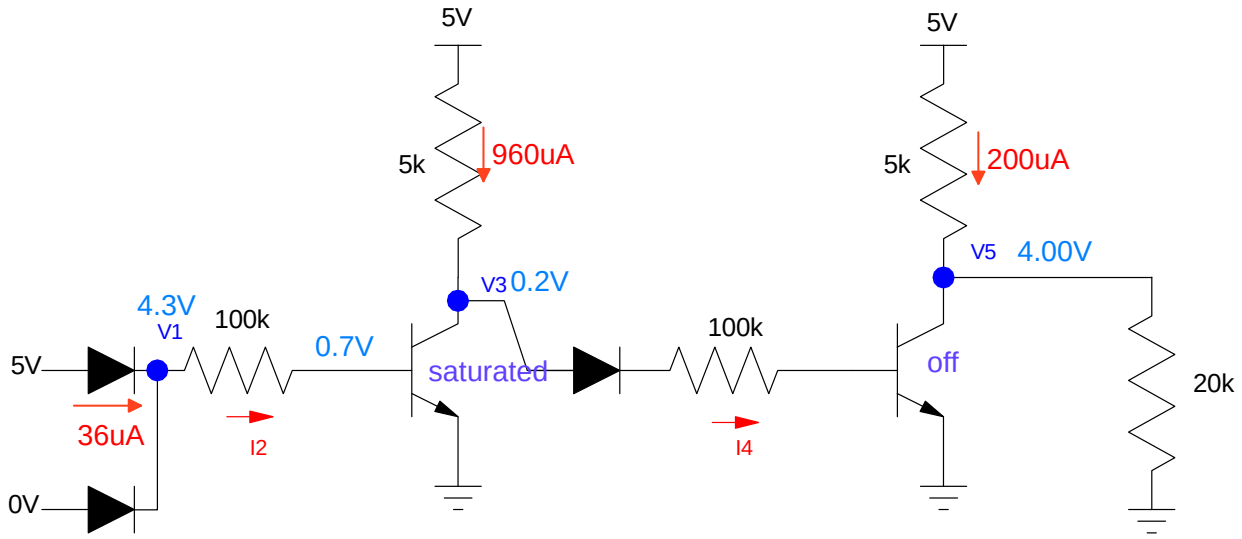
4) Determine the voltages and currents for the following DTL AND gate. Assume 3904 transistors (from problem #1)



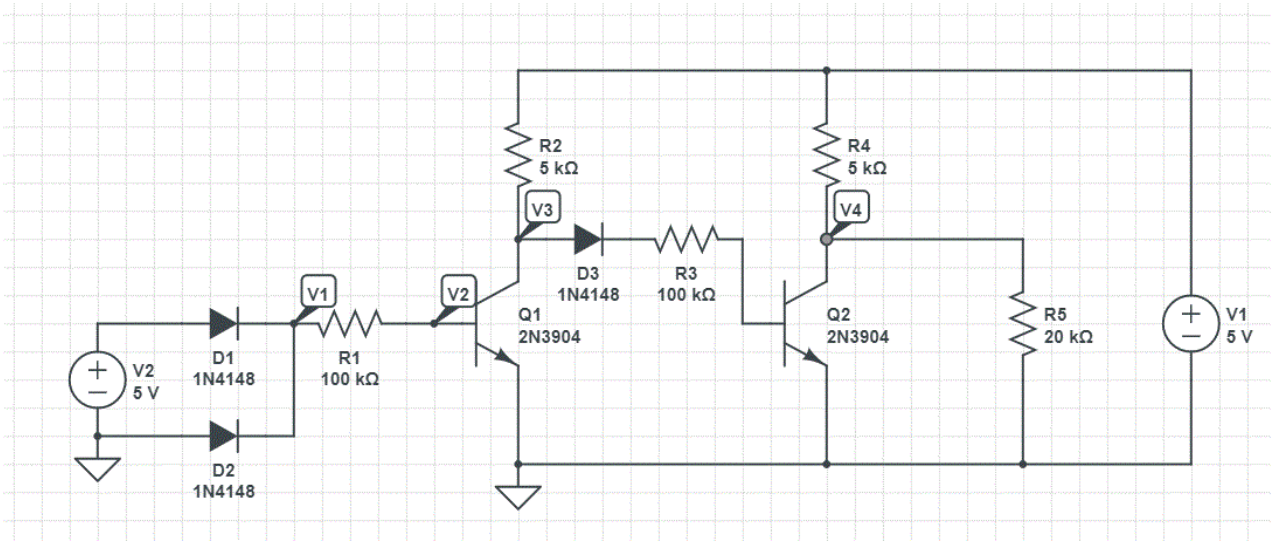
Transistor T2 is saturated

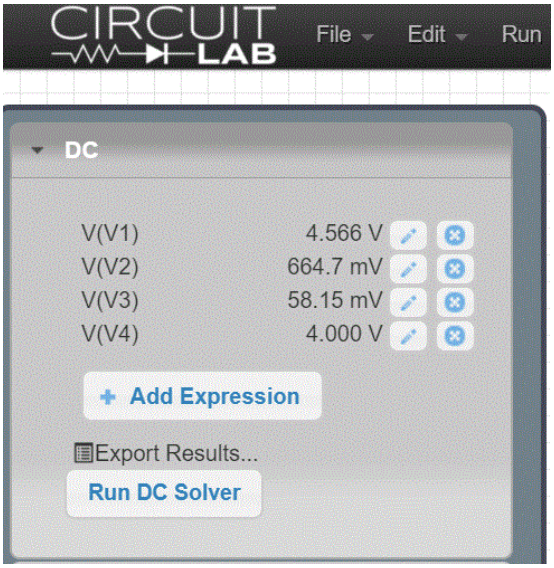
$$\beta I_b = 3.6mA > 958\mu A$$

5) Determine the voltages and currents for the following DTL OR gate. Assume 3904 transistors



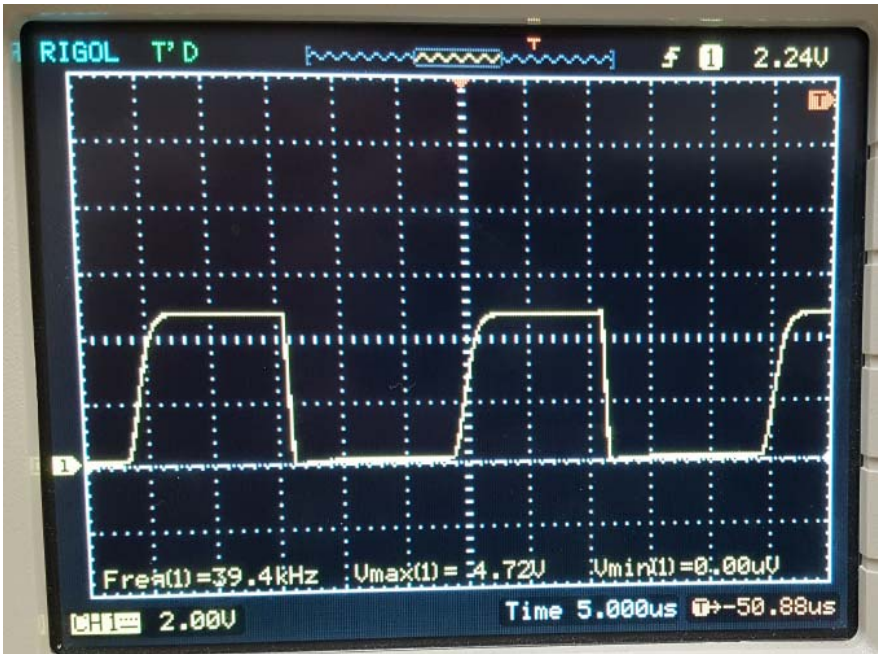
6) Check your analysis for problem #5 (DTL OR) in PartSim (or similar program)



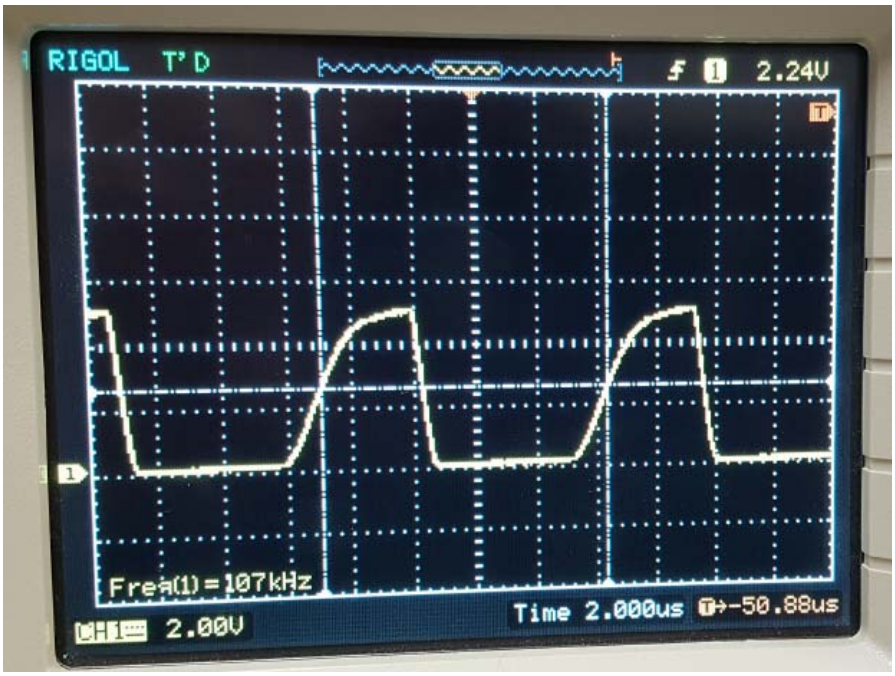


7) (Lab): Build a DTL OR gate in lab. Measure

- The votlages when the input is { 0V, 0V },
- The votlages when the input is { 0V, 5V }, and
- The maximum frequency the logic gate can respond to (apply a square wave at the input)



"True" = 4.72V, "False" = 0.00V



Maximum Frequency = 107kHz (approx)

TTL Logic

8) Determine the voltages for the following TTL inverter. Assume 2n222 transistors.

$\beta = 100$ c to e

$\beta = 4$ e to c