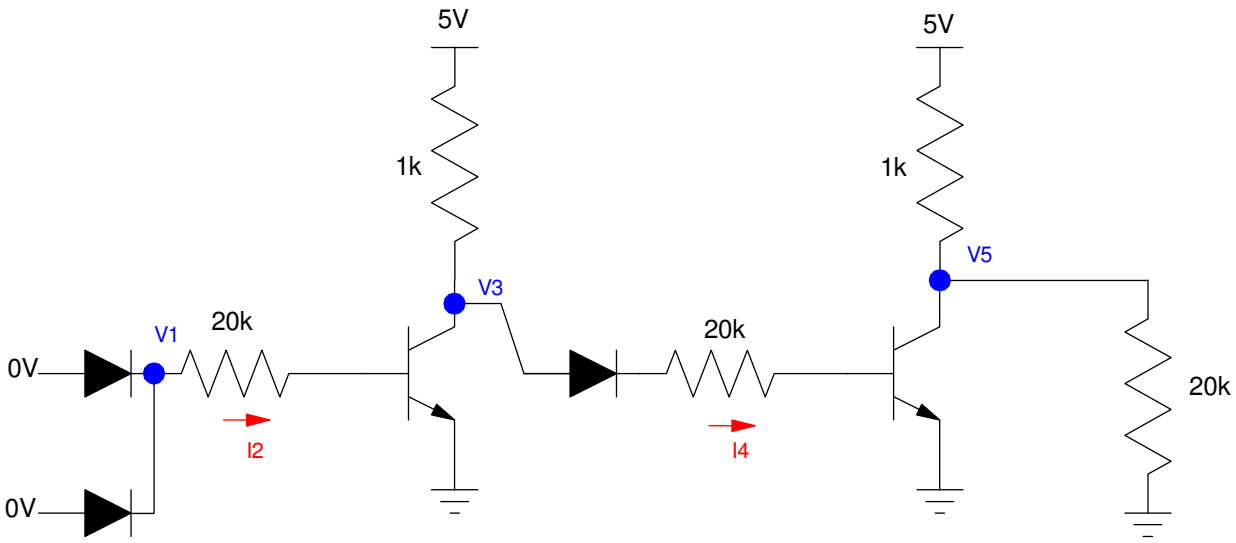
ECE 320 - Homework #8

DTL, TTL Logic, MOSFET theory. Due Monday, October 19th

DTL NOR Gate

1) Determine the voltages and currents for the following DTL OR gate

2) Simulate this circuit in CircuitLab to verify your answers for problem #1

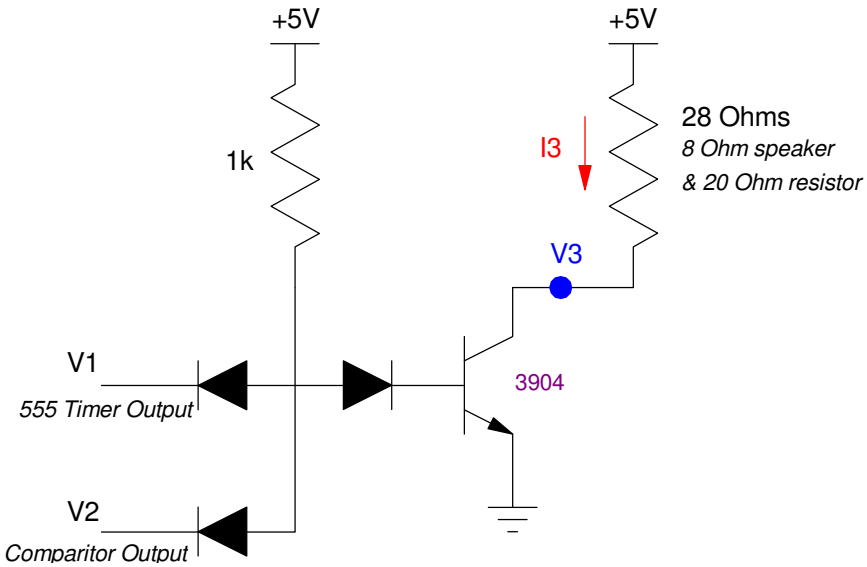


DTL NAND Gate: Open Collector Logic

The following circuit uses a DTL NAND gate to turn on a speaker when

- The output of a 555 timer is high (V1 = 5V), and
- The output of a comparitor is high (V2 = 5V)

The output is conencted directly to the collector of the transistor



3) Determine the voltage V3 and current I3 when

- V1 = V2 = 0V
- V1 = V2 = 5V
- V1 = 0V, V2 = 5V

4) Simulate this circuit for 1/30ms in CircuitLab with

- V1 = 600Hz clock signal (0V / 5V square wave)
- V2 = 60Hz clock signal (0V / 5V)

Lab (include a photo to receive credit)

5) Build this circuit using

- 0V / 5V for V1, and
- 0V / 5V for V2.

Measure the voltage you see at V3 for each case

6) Build this circuit using

- The 555 timer from homework set #5 for V1, and
- Connecting theThe comparitor from homework set #5 for V2

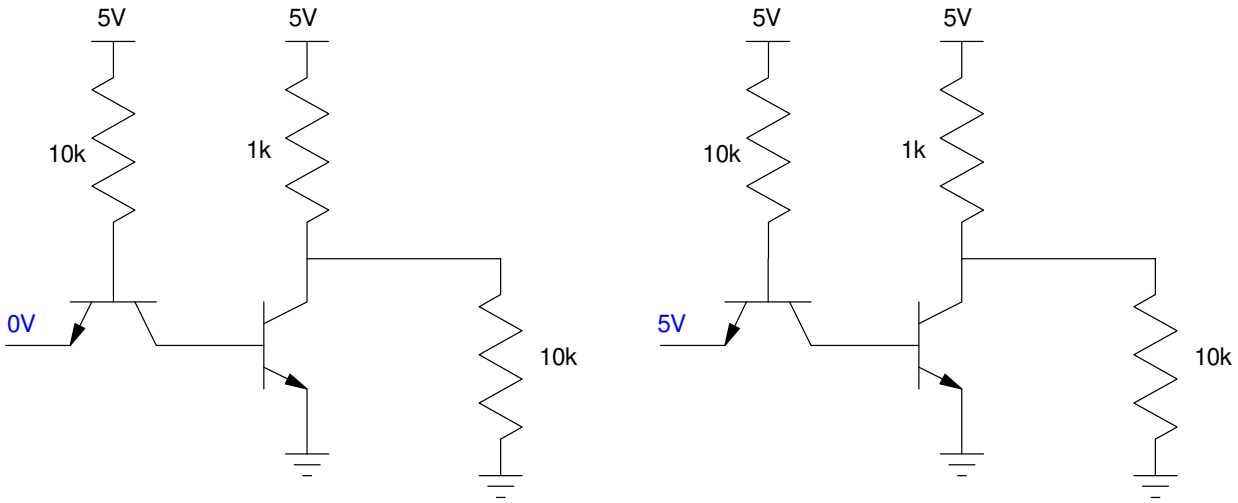
Verify that

- The speaker turns on when T > Ton and
- The speaker turns off when T < Ton

TTL Logic

7) Determine the voltages for the following TTL inverter. Assume 3904 transistors.

8) Simulate these circuits in CircuitLab and determine the voltage and currents



MOSFET

9) The VI characteristics for an n-channel MOSFET is shown on the following page. Assume Vth = 1.0V

- Determine the transconductance gain, kn
- Label the off / saturated / ohmic regions in the curve below.

10) Draw the load line and mark the operating points for Vg = { 0V, 4V, 7V }