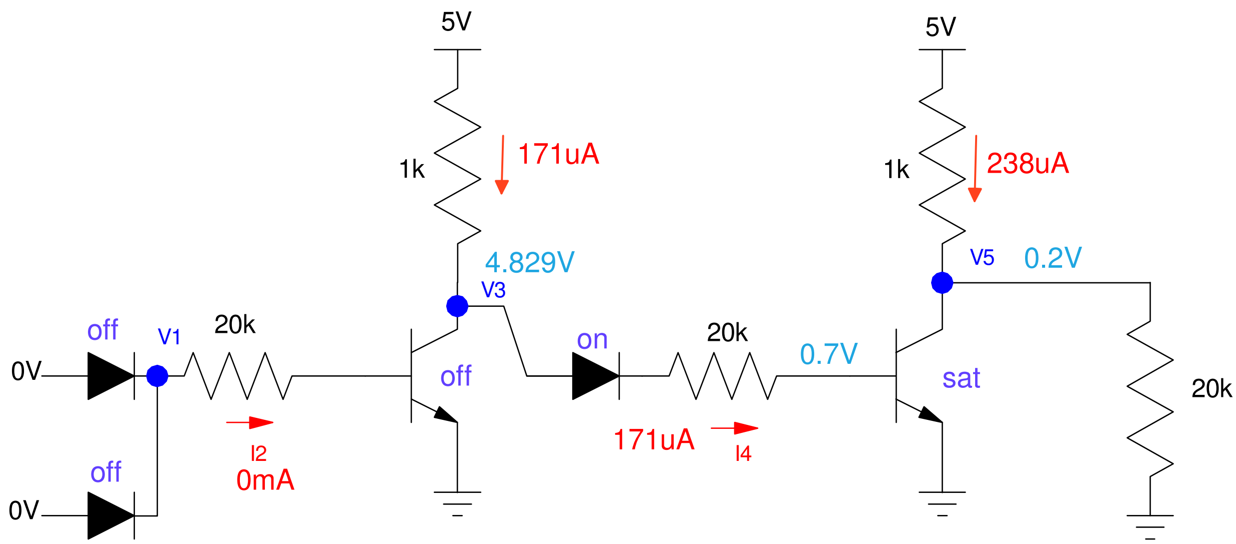
ECE 320 - Homework #8

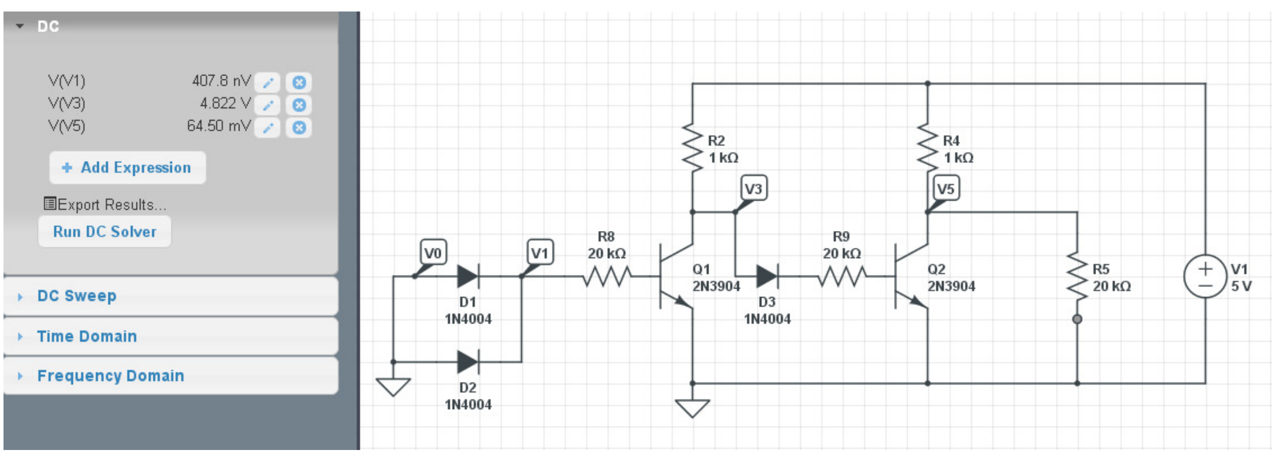
DTL, TTL Logic, MOSFET theory. Due Monday, October 19th

DTL NOR Gate

1) Determine the voltages and currents for the following DTL OR gate



2) Simulate this circuit in CircuitLab to verify your answers for problem #1



DTL NAND Gate: Open Collector Logic

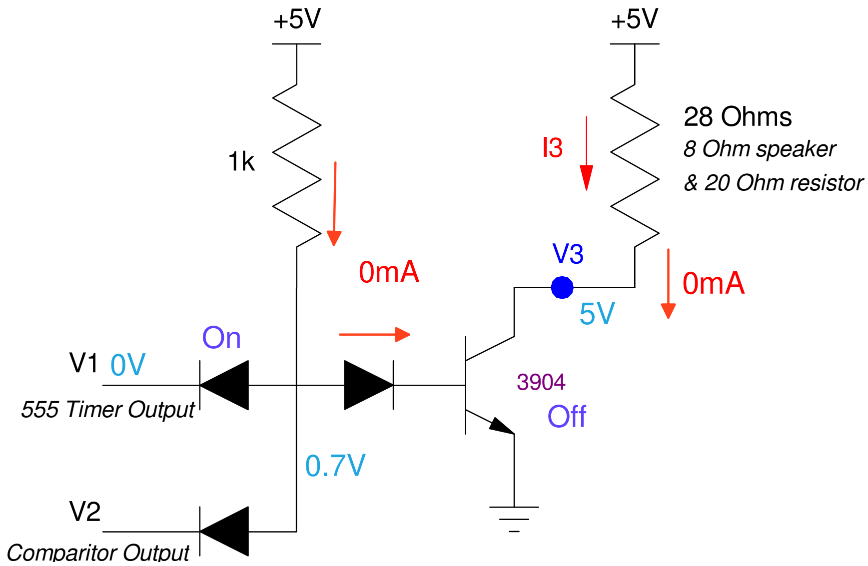
The following circuit uses a DTL NAND gate to turn on a speaker when

- The output of a 555 timer is high (V1 = 5V), and
- The output of a comparitor is high (V2 = 5V)

The output is conencted directly to the collector of the transistor

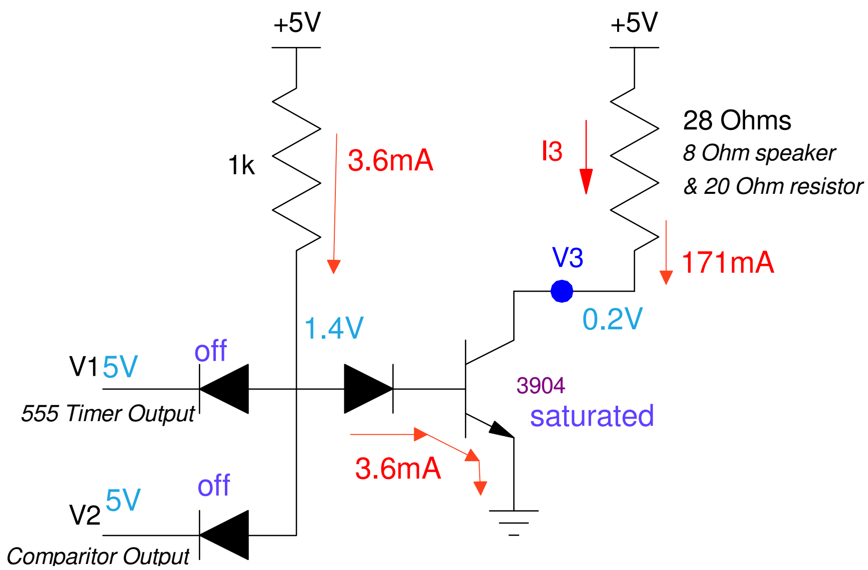
3) Determine the voltage V3 and current I3 when

- V1 = 0V
- V2 = any



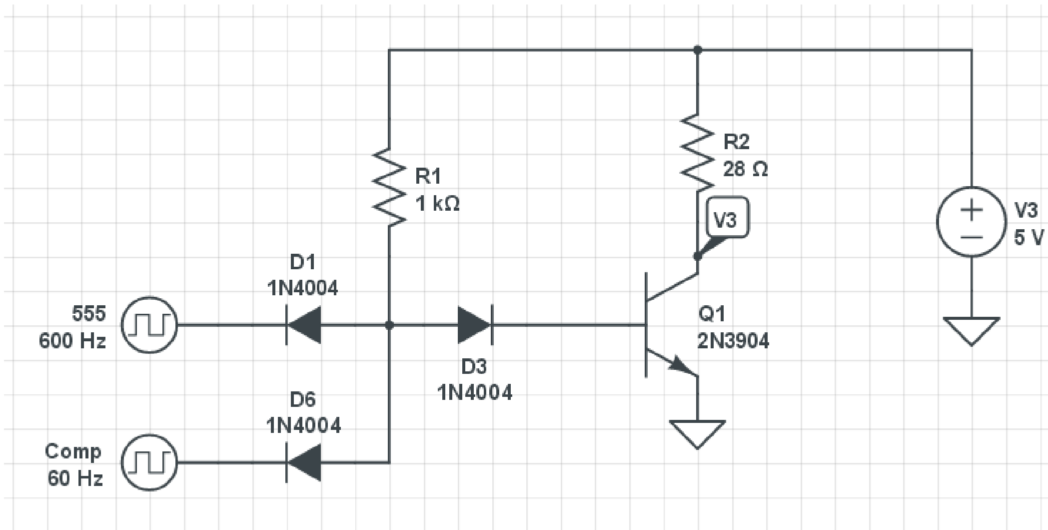
Case 2:

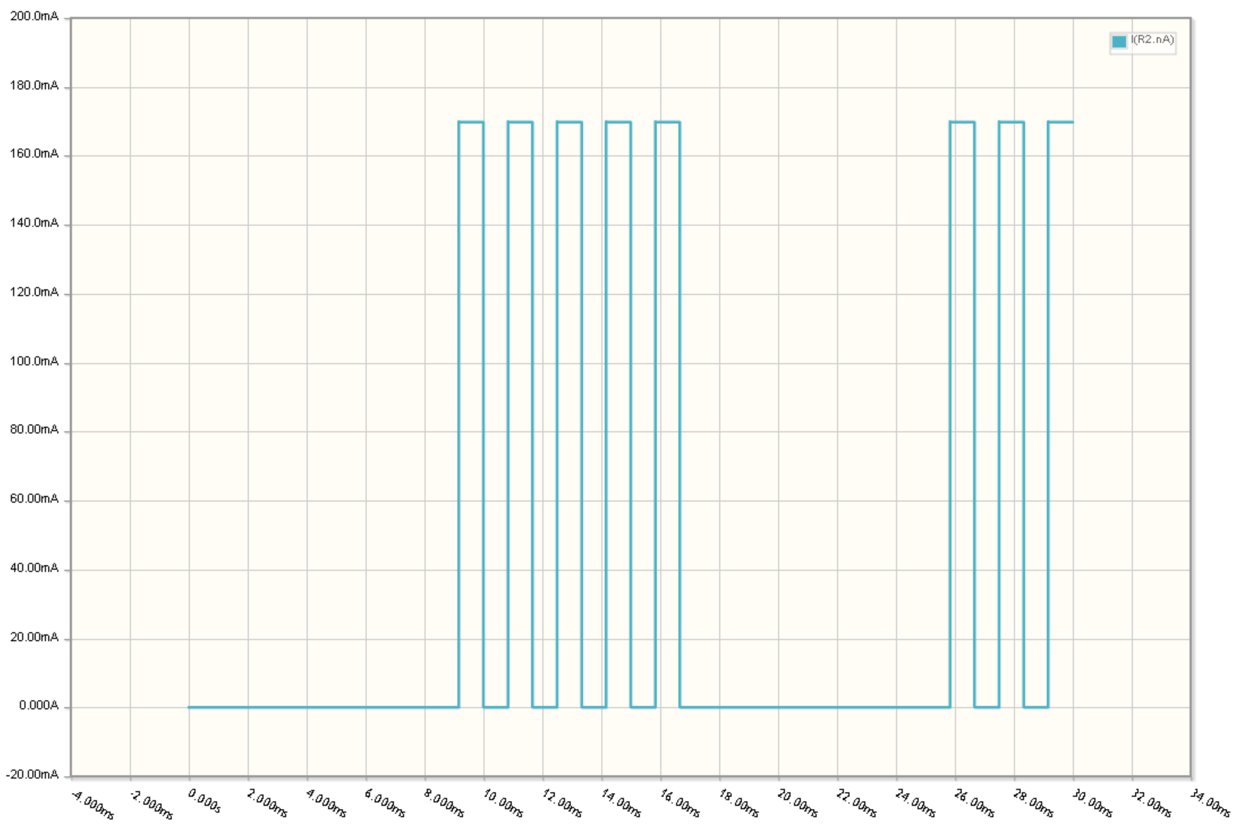
- V1 = V2 = 5V



4) Simulate this circuit for 1/30ms in CircuitLab with

- V1 = 600Hz clock signal (0V / 5V square wave)
- V2 = 60Hz clock signal (0V / 5V)

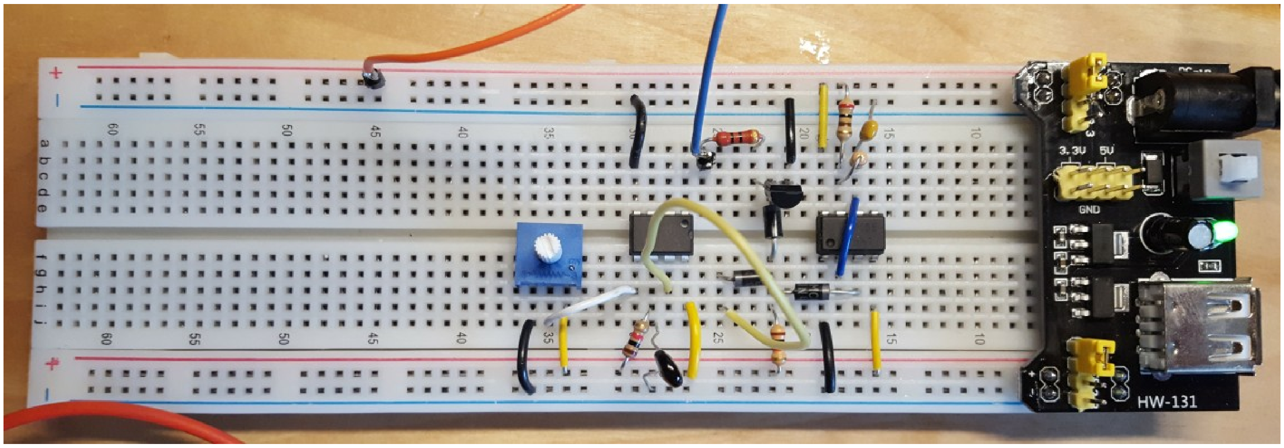


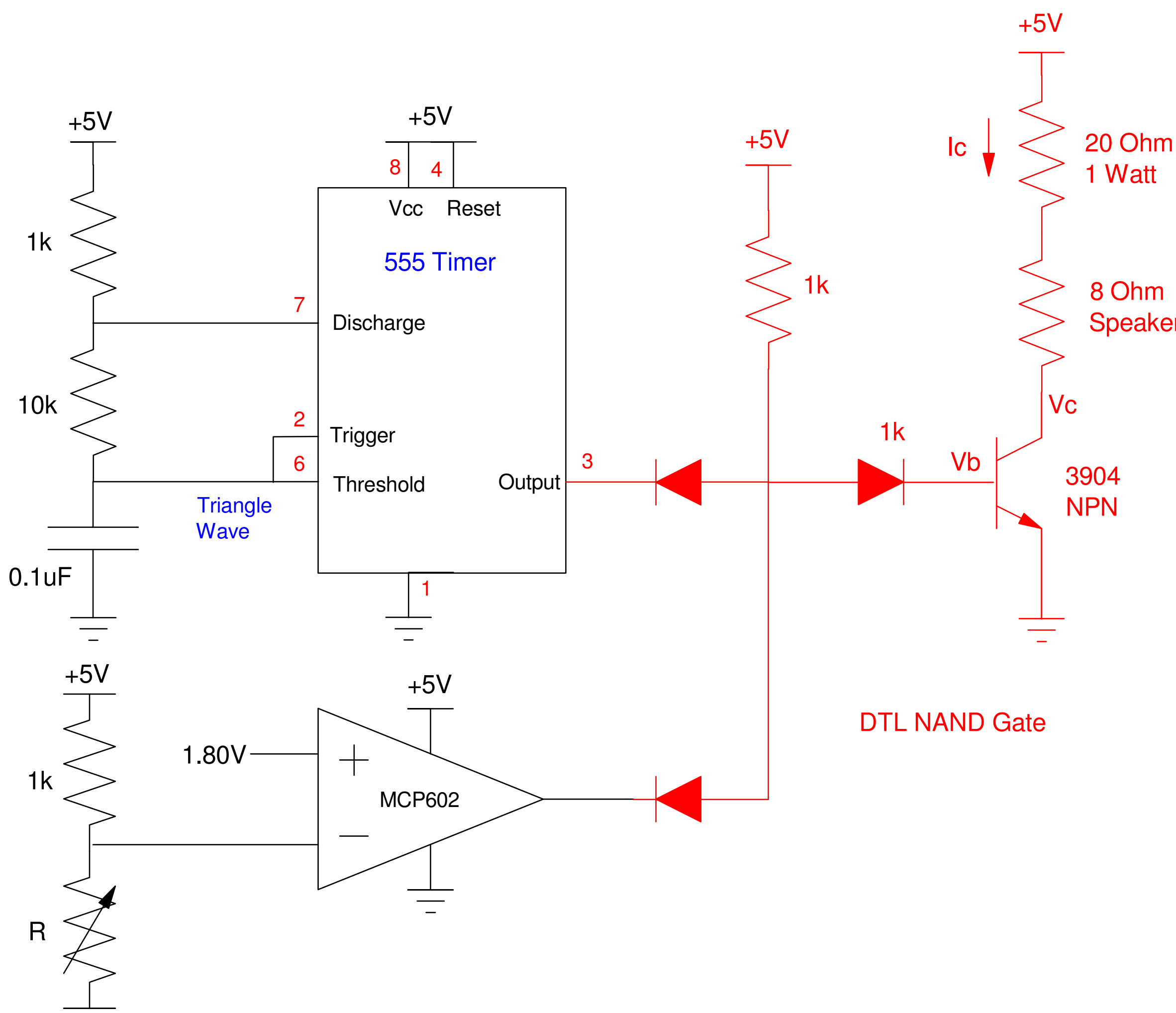


Current through the Speaker: I(R2)

Lab (include a photo to receive credit)

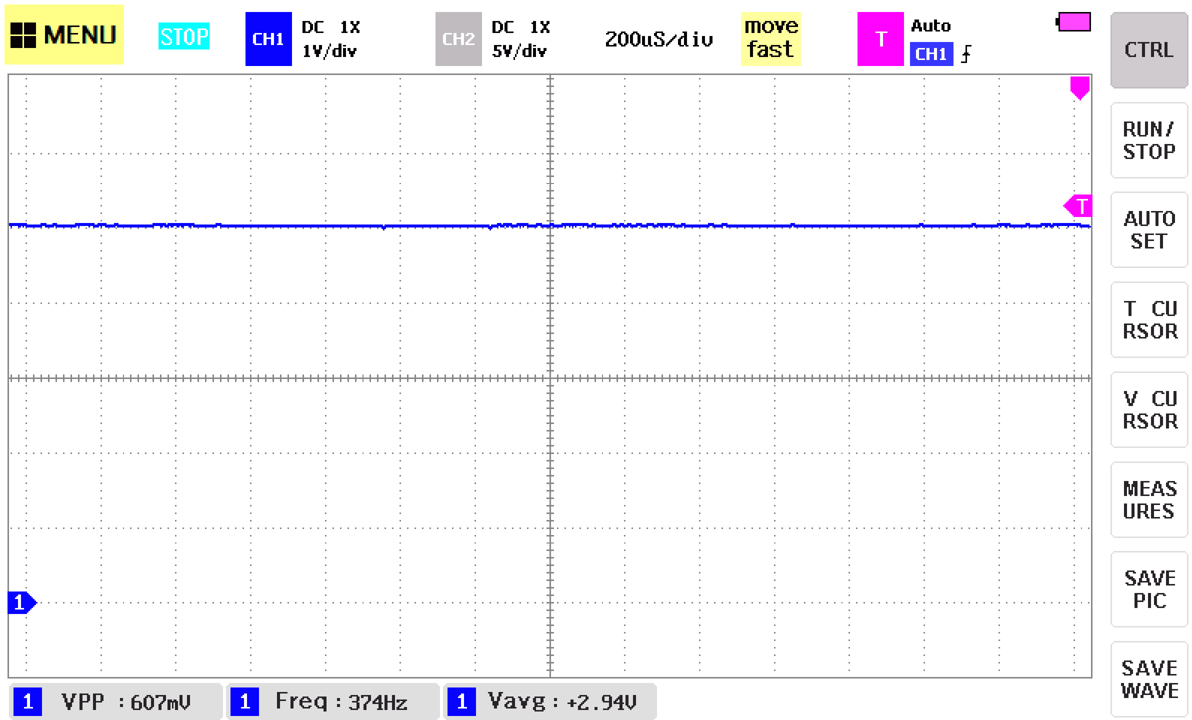
5) Build this circuit and measure the voltage you see at V3 for each case





Case 1: 0V applied to diode #2

- The transistor is always off
- Vc = 5V (transistor is off)



Case 2: 5V applied to diode #2

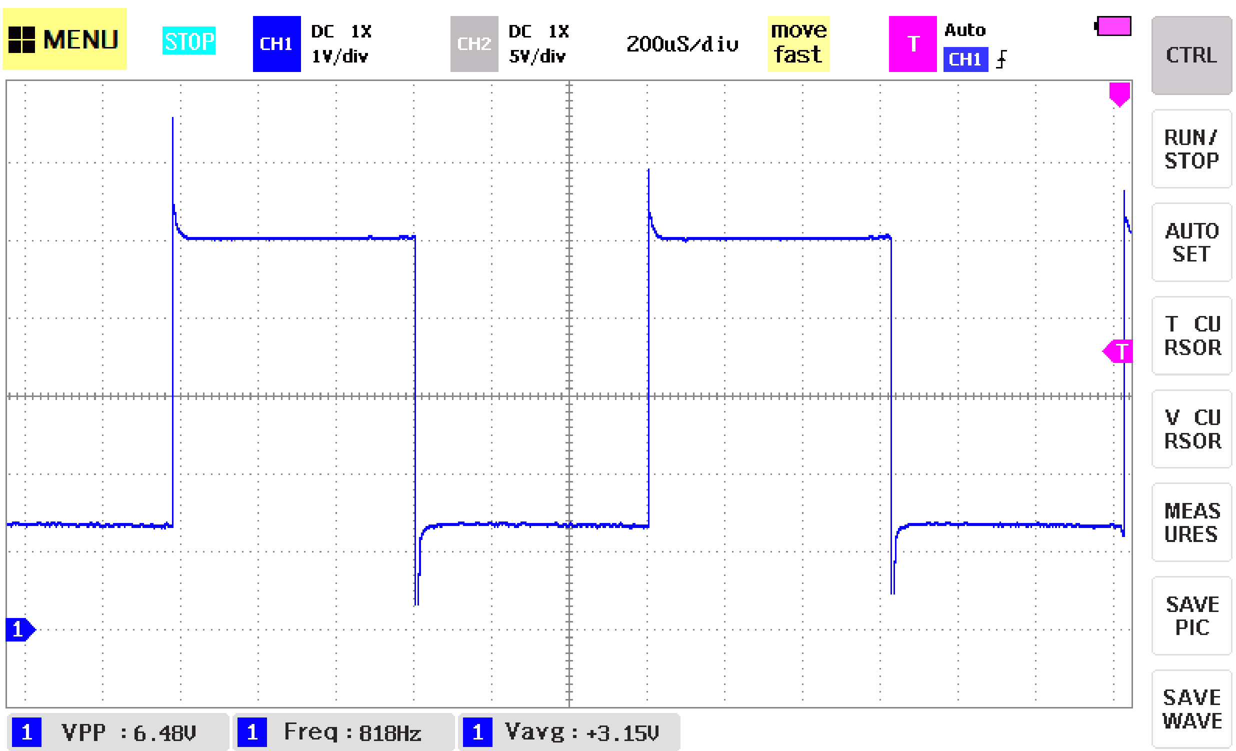
- Vc = 5V when the 555 timer outputs 0V (transistor off)
- Vc = 1.2V when the 555 timer outputs 5V (transistor is active mode)

Apparently, the current gain is less than 100 and I need more base current

$$I_c = \left(\frac{5V-1.2V}{28\Omega}\right) = 136mA$$

$$I_b = \left(\frac{5V-0.7V}{1k}\right) = 4.3mA$$

$$\beta = \frac{I_c}{I_b} = \frac{136mA}{4.3mA} = 31.6$$



6) Build this circuit using

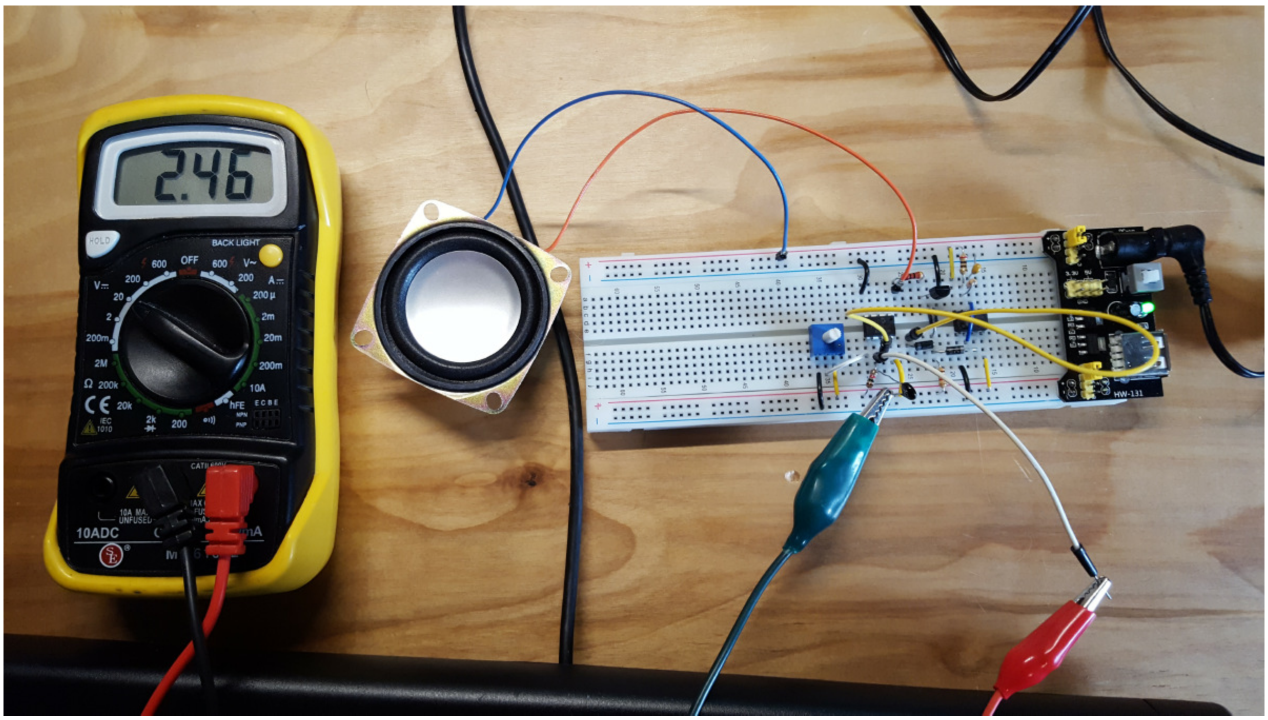
- The 555 timer from homework set #5 for V1, and
- Connecting theThe comparitor from homework set #5 for V2

Verify that

- The speaker turns on when T > Ton and
- The speaker turns off when T < Ton

Setting the comparitor to turn on at 1.80V

- Speaker turns on when Vr < 1.80V
- Speaker turns off when Vr > 1.83V

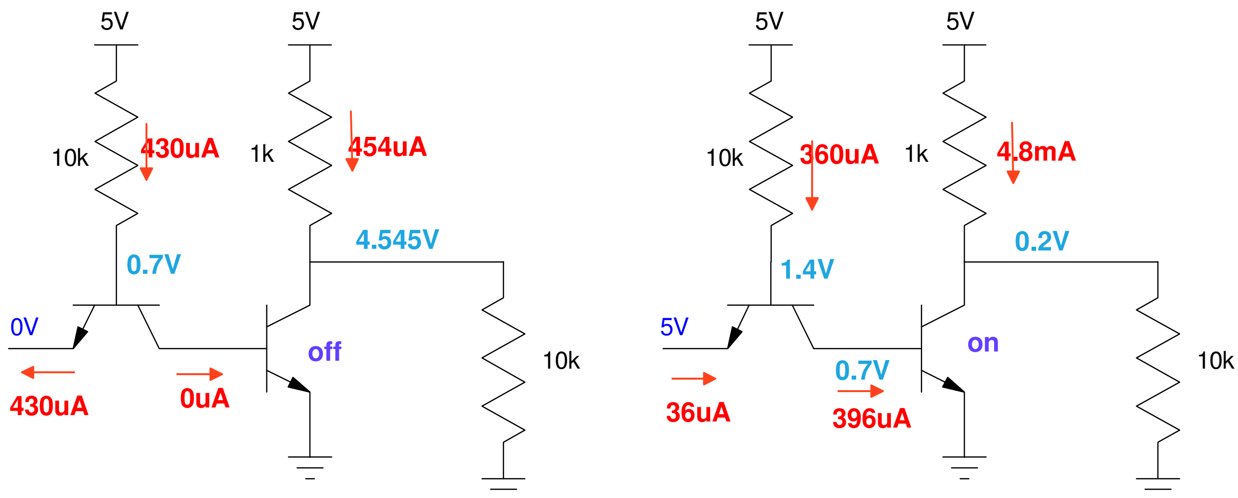


Measuring the voltage where the speaker turns on and off

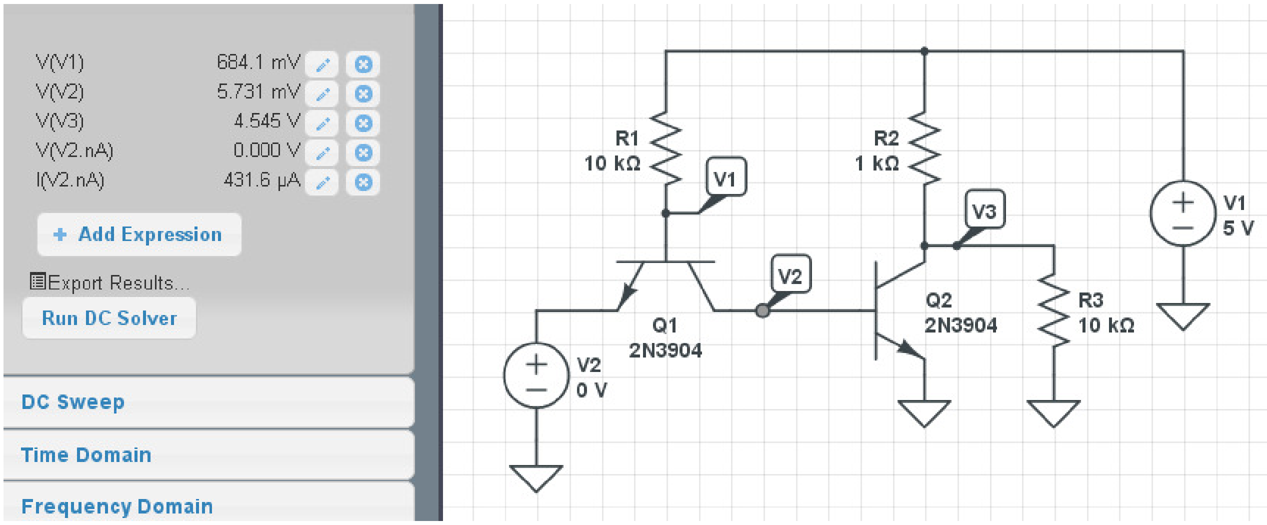
TTL Logic

7) Determine the voltages for the following TTL inverter. Assume

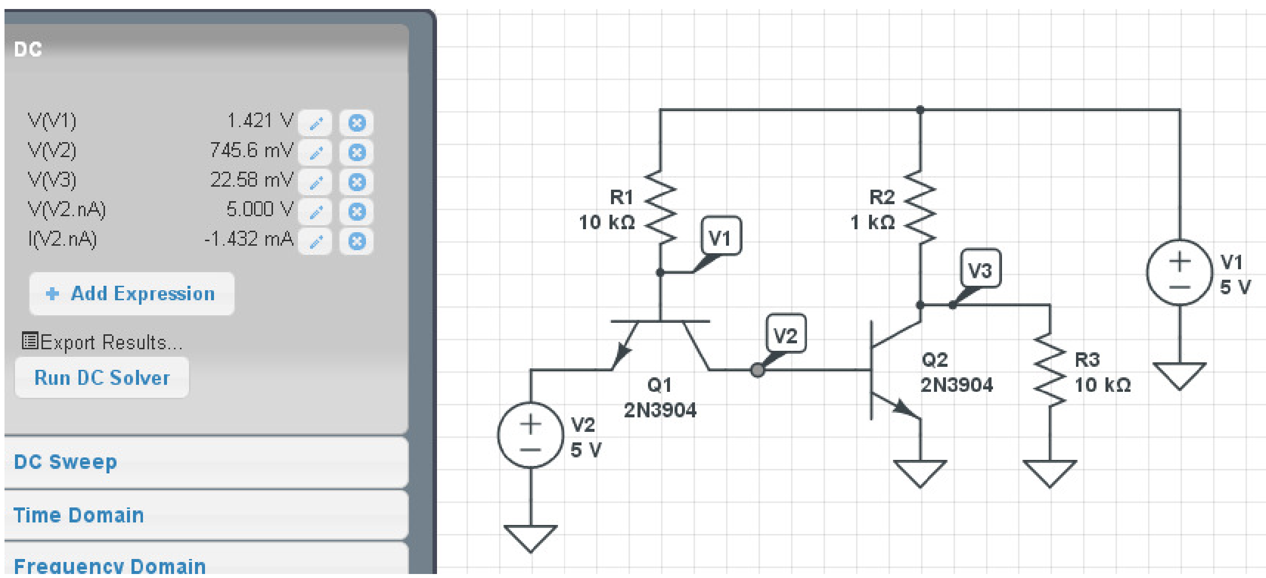
- 3904 transistors.
- Current gain = 0.1 when used backwards



8) Simulate these circuits in CircuitLab and determine the voltage and currents



Case 1: 0V in produces 5V out (actually 4.545V due to loading)



Case 2: 5V in produces 0V out (22.58mV actually)
note: Ic = 4 Ib. Q1 has a gain of 4.00 when used backwards

MOSFET

9) The VI characteristics for an n-channel MOSFET is shown on the following page. Assume Vth = 1.0V

- Determine the transconductance gain, kn
- Label the off / saturated / ohmic regions in the curve below.

kn: Point A (Ohmic region)

$$I_{ds} = k_n\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds}$$

$$4mA = k_n\left(5V - 1V - \frac{2V}{2}\right)2V$$

$$k_n = 666.7\frac{\mu A}{V^2}$$

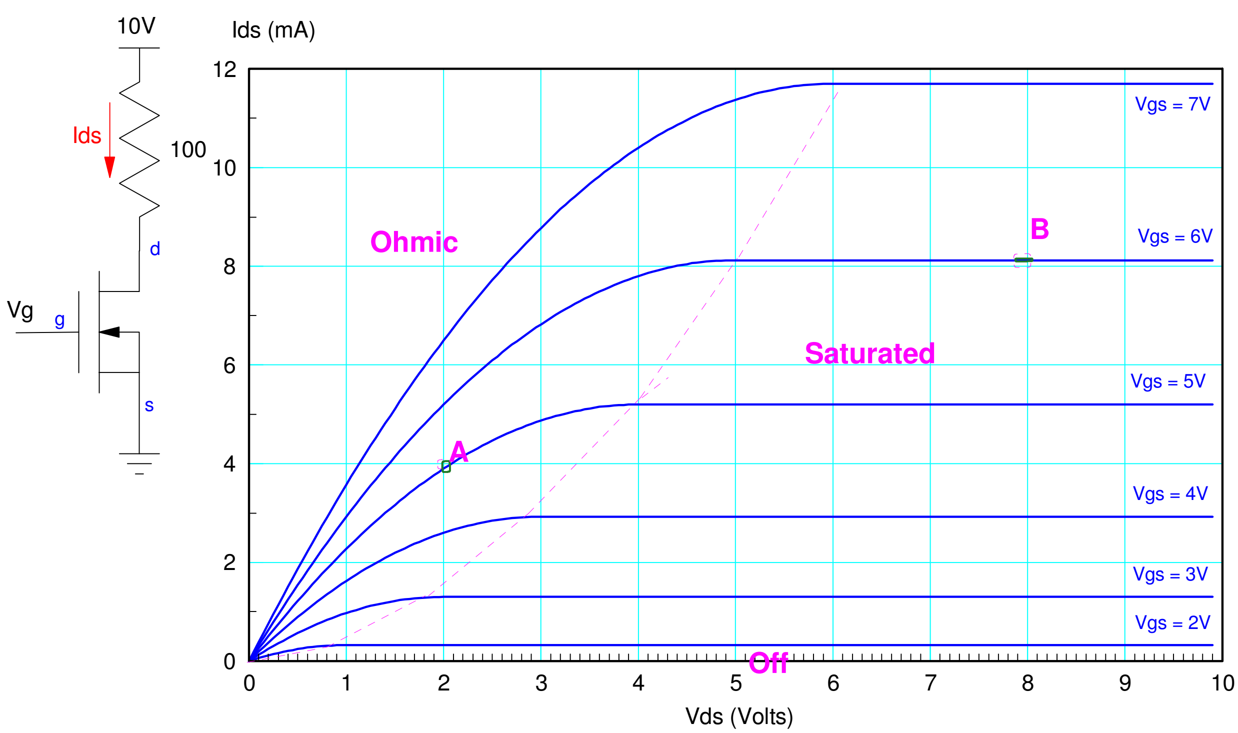
Point B (Saturated Region)

$$I_{ds} = \frac{k_n}{2}(V_{gs} - V_{th})^2$$

$$8.1mA = \frac{k_n}{2}(6V - 1V)^2$$

$$k_n = 648\frac{\mu A}{V^2}$$

The two answers should be the same (errors in reading the graph result in the slight difference)



10) Draw the load line and mark the operating points for Vg = { 0V, 4V, 7V } (change R to 1000 Ohms. Otherwise it's off the chart)

0V:

- Vds = 10V
- Ids = 0V
- Off region

4V:

- Vds = 7V
- Ids = 3mA
- Saturated Region

7V:

- Vds = 2.3V
- Ids = 7.5mA
- Ohmic Region