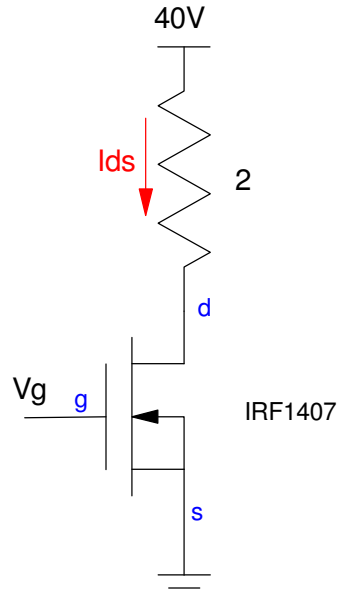
ECE 320 - Homework #9

MOSFET switch, CMOS logic. Due Monday, October 26th

MOSFET Switch



One of the MOSFET's that CircuitLab has is an IRF1047. It's specifications are

- max(Ic) = 100A continuous
- Vgs(th) = 4V (max)
- Rds = 7.8mOhm @ Ids = 78A @ Vgs = 10V
- $0.53 each

1) Determine the transconductance gain, kn, for this MOSFET. Assume Vtn = 4.00V

In the Ohmic region:

$$V_{ds} = (7.8m\Omega)(78A) = 0.608V$$

$$I_{ds} = k_n\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds}$$

$$78A = k_n\left(10 - 4 - \frac{0.608}{2}\right)0.608$$

$$k_n = 22.509\ \frac{A}{V^2}$$

2) Determine the votlages and currents for the following circuit when Vg = 5V

Assume Ohmic:

$$I_{ds} = k_n\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds}$$

$$I_{ds} = 22.509\left(5 - 4 - \frac{V_{ds}}{2}\right)V_{ds}$$

$$V_{ds} + 2I_{ds} = 40$$

no solution.

Assume saturated

$$I_{ds} = \frac{k_n}{2}(V_{gs} - V_{th})^2$$

$$I_{ds} = \frac{22.509}{2}(5 - 4)^2$$

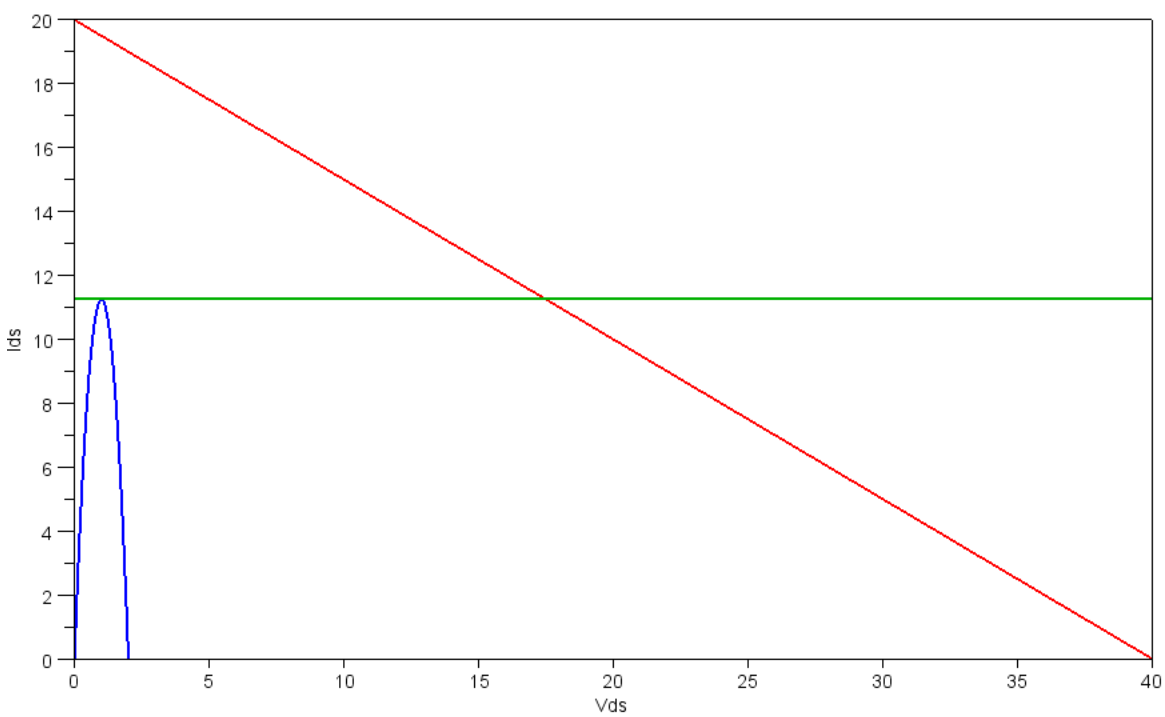
$$I_{ds} = 11.255A$$

$$V_{ds} = 40 - 2I_{ds}$$

$$V_{ds} = 17.491V$$

Check

$$V_{ds} > V_{gs} - V_{th}$$

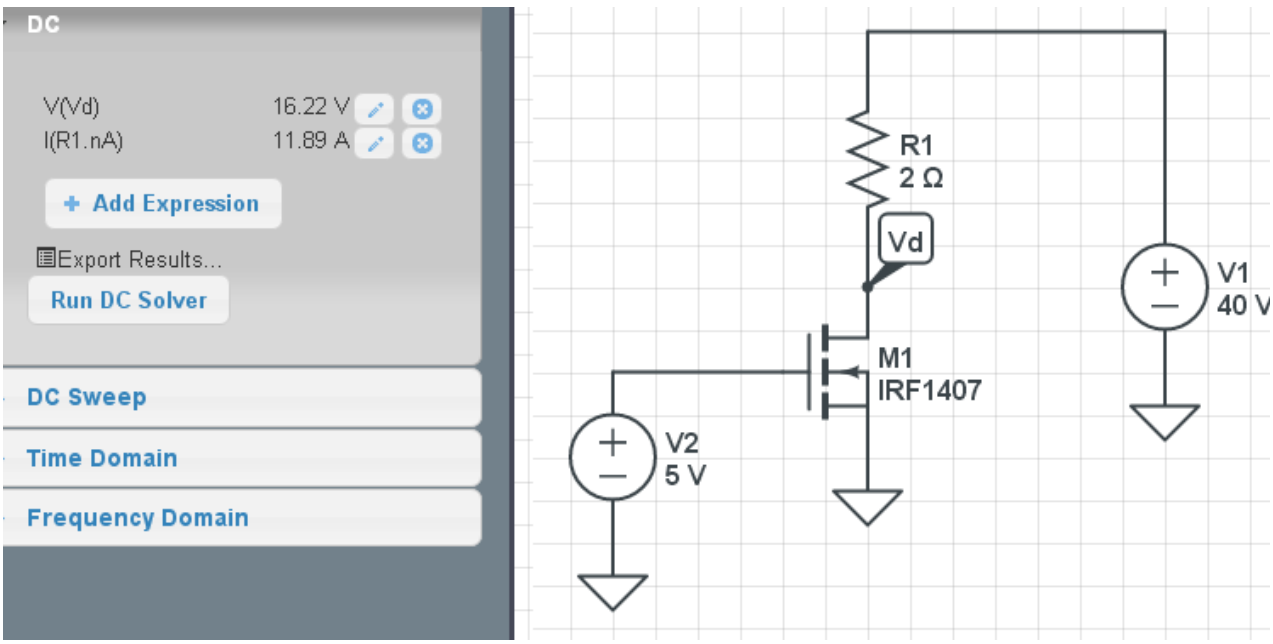


Load Line (red), Ohmic Model (blue), and Saturated Model (green)

matlab code:

```
Vds = [0:0.01:40]';

I1 = 22.509*(5-4-Vds/2).*Vds;

I2 = (40 - Vds)/2;

I3 = 0*Vds + max(I1);

plot(Vds,I1,'b',Vds,I2,'r',Vds,I3,'g');
xlabel('Vds');
ylabel('Ids');
```

Check your result in CircuitLab



	Vds	Ids
Calcualted	17.49V	11.26A
Simulated	16.22V	11.89A

3) Determine the votlages and currents for the following circuit when Vg = 10V

- Check your result in CircuitLab

Assume Ohmic

$$I_{ds} = k_n\left(V_{gs} - 4 - \frac{V_{ds}}{2}\right)V_{ds}$$

$$I_{ds} = 22.509\left(10 - 4 - \frac{V_{ds}}{2}\right)V_{ds}$$

$$V_{ds} + 2I_{ds} = 40$$

Solving

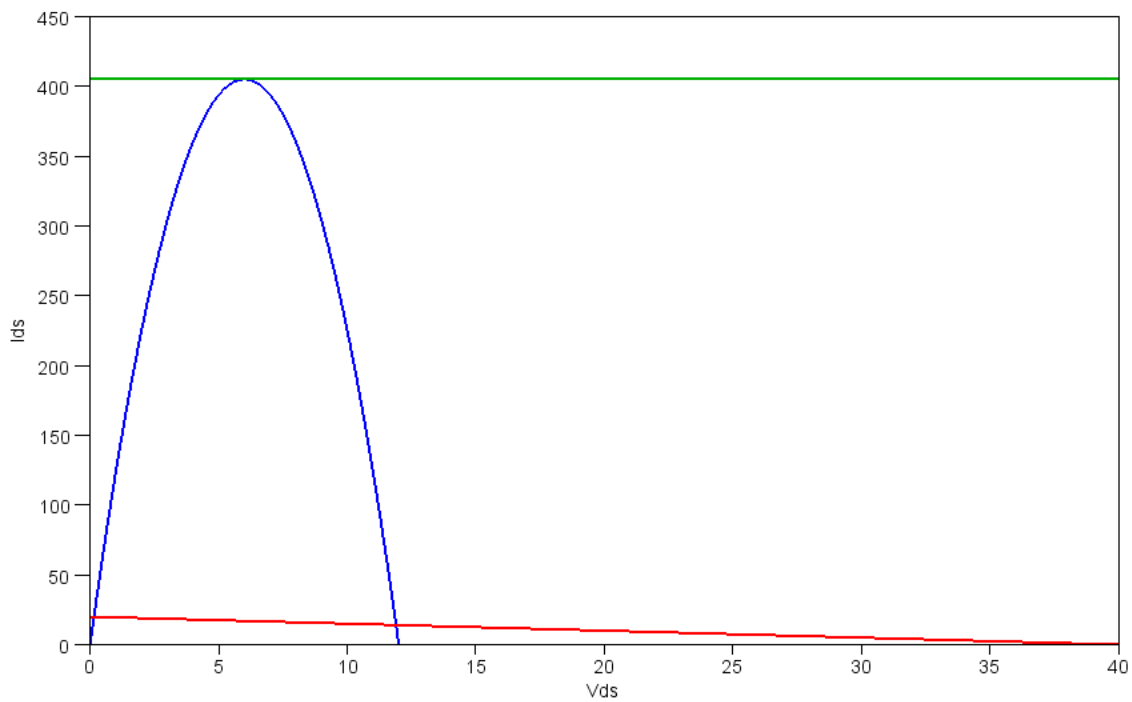
$$V_{ds} = 149.4mV$$

$$I_{ds} = 19.925A$$

$$R_{ds} = \frac{V_{ds}}{I_{ds}} = 77.6m\Omega$$

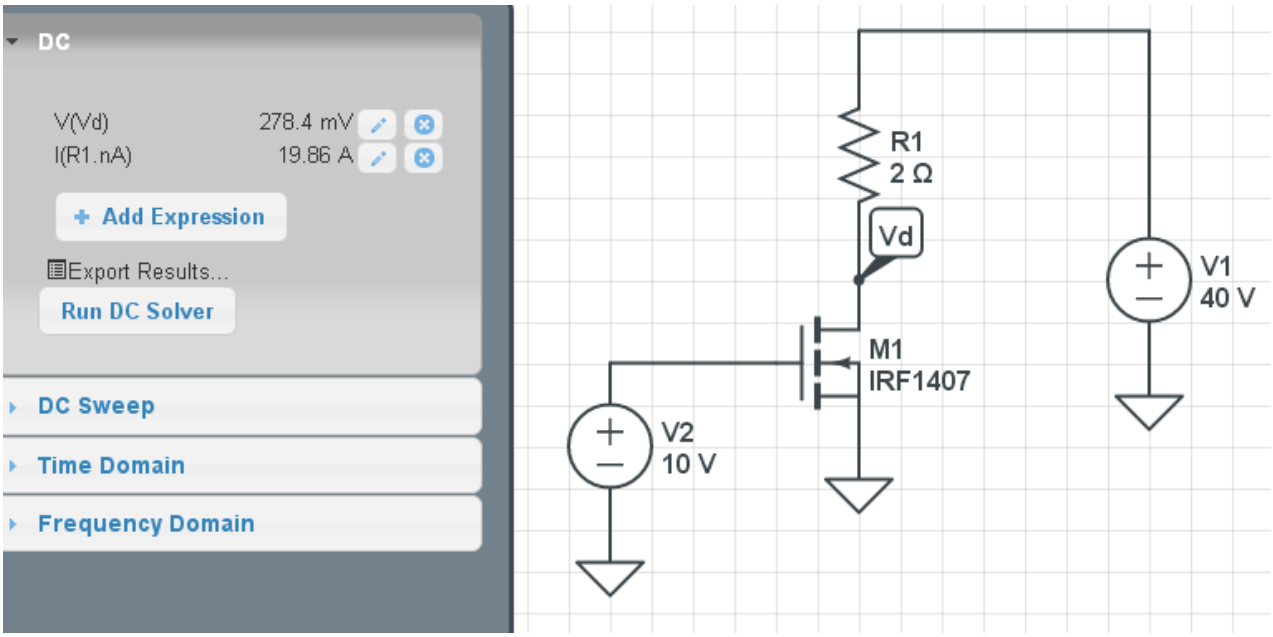
Matlab Code

```
Vds = [0:0.01:40]';
I1 = 22.509*(10-4-Vds/2).*Vds;
I2 = (40 - Vds)/2;
I3 = 0*Vds + max(I1);
plot(Vds,I1,'b',Vds,I2,'r',Vds,I3,'g');
xlabel('Vds');
ylabel('Ids');
```



Load Line (red), Ohmic Model (blue), Saturated Model (green)

In CircuitLab



	Vds	Ids
Calcualted	149mV	19.93A
Simulated	278mV	19.86A

CMOS Logic

4) Design a CMOS gate to implement the function: f(A, B, C, D)

Circle the zeros (also works if you circle the ones)

AB \ CD	00	01	11	10
00	1	0	0	0
01	1	1	0	1
11	x	x	x	x
10	1	1	x	x

$$\overline{Y} = CD + \overline{B}C + \overline{A}\overline{B}C$$

$$Y = \left(\overline{C} + \overline{D}\right)\left(B + \overline{C}\right)\left(A + B + \overline{C}\right)$$