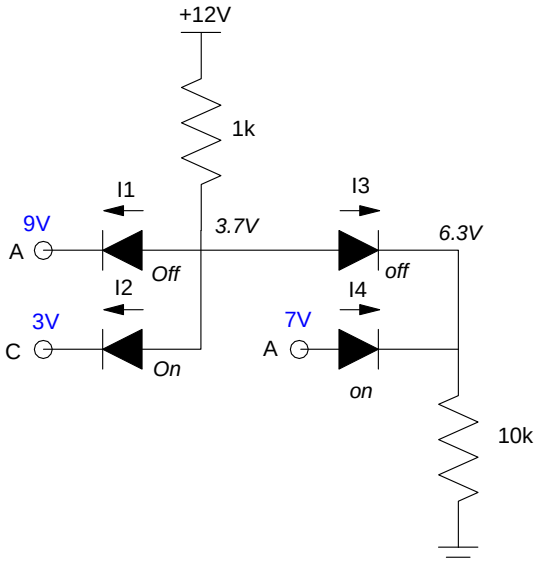
ECE 320 - Solution to Homework #4

Max/Min, AC to DC, DC to DC Converters. Due Monday, February 8tht

Assume ideal silicon diodes with Vf = 0.7V.

Max / Min:

1) Determine the voltages for the following circuit.



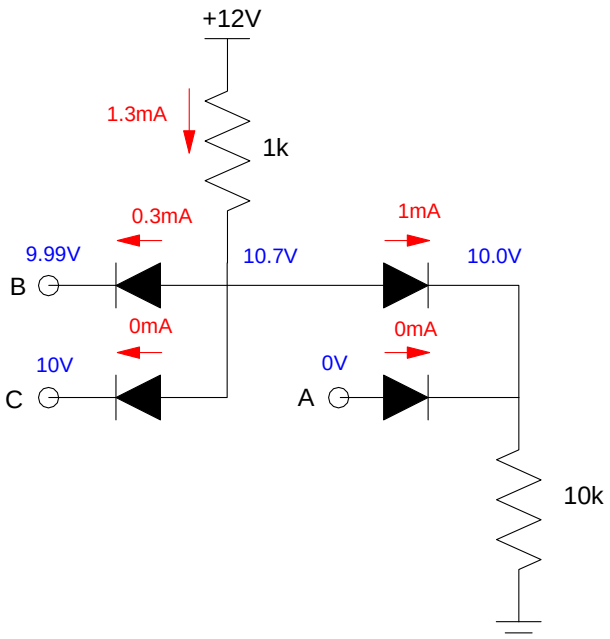
Problem 1

2) Design a circuit to meet the following requirements:

Inputs: A, B, C, 0 .. 10V signals, capable of 20mA

Outputs: Y, capable of driving 1uA

Relationship: Y = A+BC = max(A, min(B, C))



Check if the circuit works: Take the worst case - both B and C are 10V, A is 0V. Is there enough current? (shown above)

answer: Just barely: 0.3mA remains to flow through diode B.

AC to DC Converters:

3) Assume L = 0. Design an AC to DC converter to drive a 100mA load with a ripple less than 500mVpp.

Input: 15Vp, 60Hz sine wave, capable of driving 1A

Output: 0 .. 100 mA load

Relationship: The output should be a DC signal with less than 500mVpp ripple. (Target = 500mVpp with a load of 100mA).

Rload:

$$R = \frac{14.3V}{100mA} = 143\Omega$$

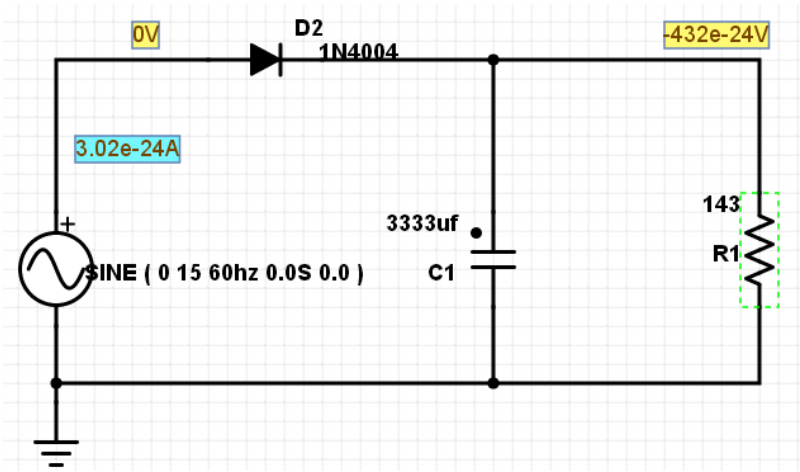
C:

$$I = C\frac{dV}{dt}$$

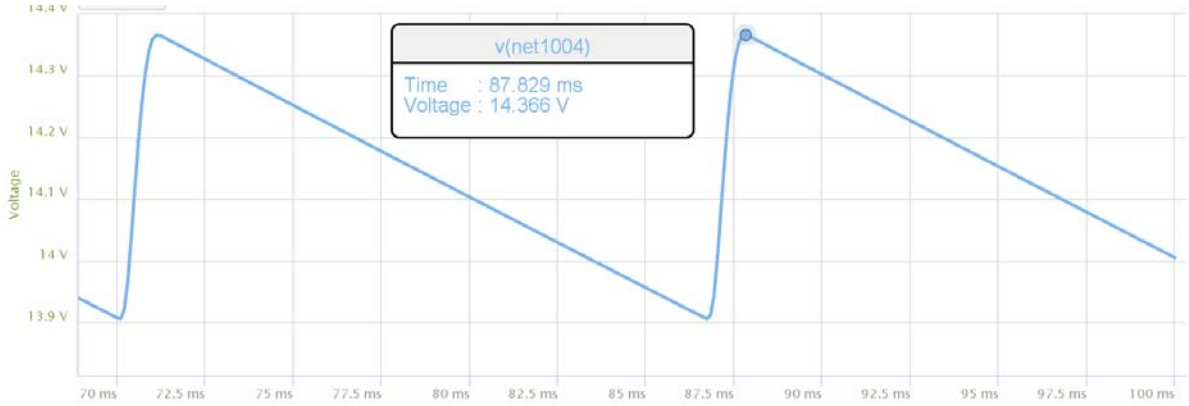
$$100mA = C\frac{500mV}{1/60s}$$

$$C = 3,333\mu F$$

Check in PartSim:

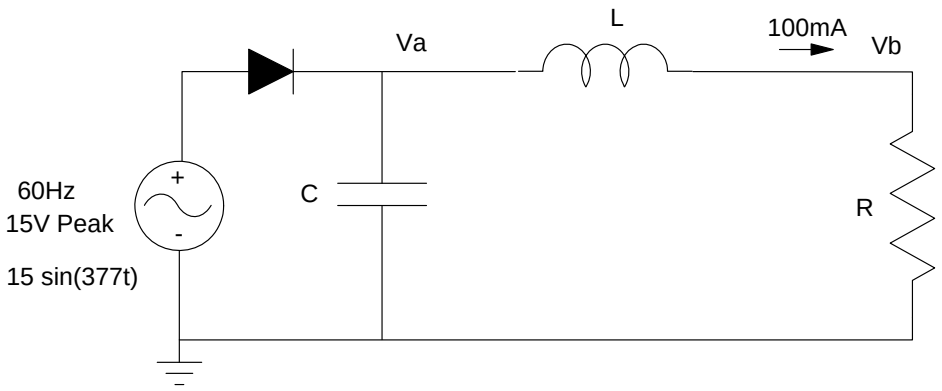


Capacitor added to reduce the ripple to 500mV (Diode is a Vendor Parts / Fairchild / Rectifier Diode / 1N4004)



Voltage at the load: 13.906V < Vout < 14.366V (460mVpp)

4) Modify your design for problem #3 to include an inductor so that the ripple is reduced to 100mVpp with a load of 100mA.



Problem 3 & 4

The RL circuit form a votlage divider. The gain is

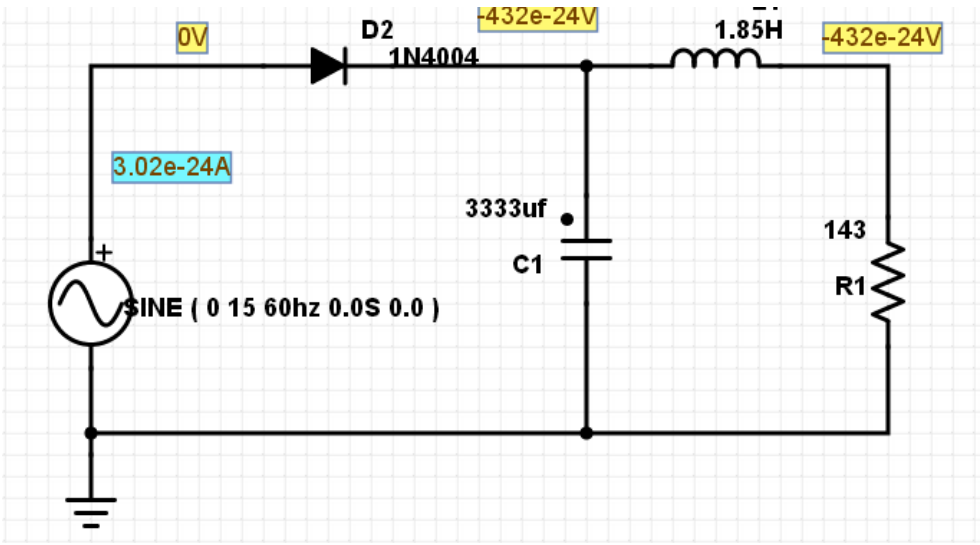
$$V_b = \left(\frac{R}{R+j\omega L}\right) V_a$$

- The ripple is at 60Hz (377 rad/sec).
- The amplitude of the ripple is Va = 500mVpp (from problem 3)
- The output should be 100mVpp (requirement)

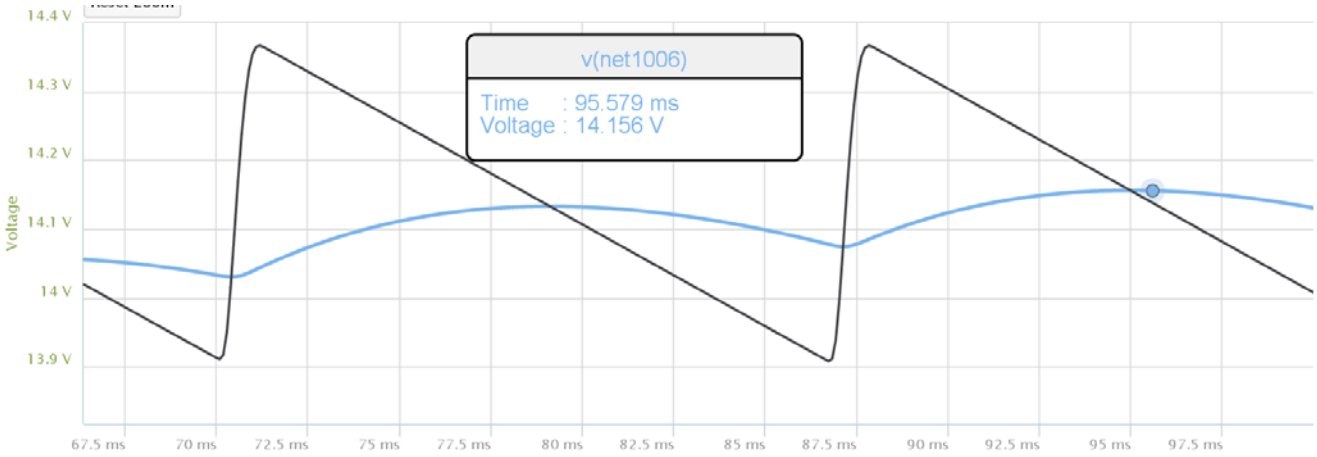
$$100mV_{pp} = \left(\frac{143}{143+j377L}\right) 500mV_{pp}$$

$$|143 + j\omega L| = 715\Omega$$

$$L = 1.85H$$



Inductor added to reduce the ripple to 100mV



Vc (black) and Vload (blue). 14.074V < Vload < 14.156V (82mVpp)

DC to DC Converter (Buck converter)

Design a circuit to convert 15VDC to 8VDC.

5) Assume C = 0. Find R, L, and the duty cycle with a switching frequency of 1kHz to convert 15VDC to 8VDC with a ripple of 500mVpp when the load is 100mA.

Duty cycle = 8/15

For the ripple to be 500mV

$$V_L = \left(\frac{R}{R+j\omega L}\right) V_{in}$$

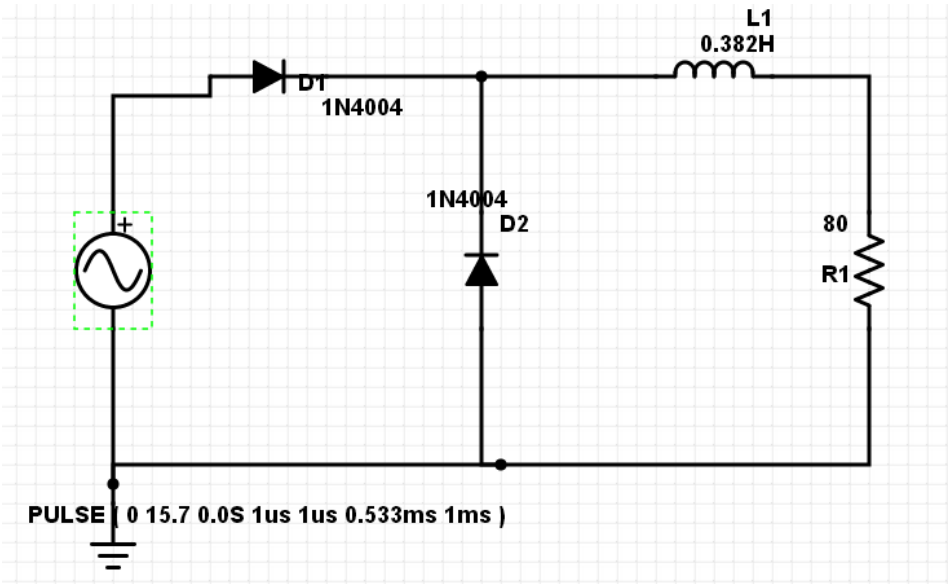
The input has a ripple of 15Vpp

R = 80 Ohms for 100mA @ 8V

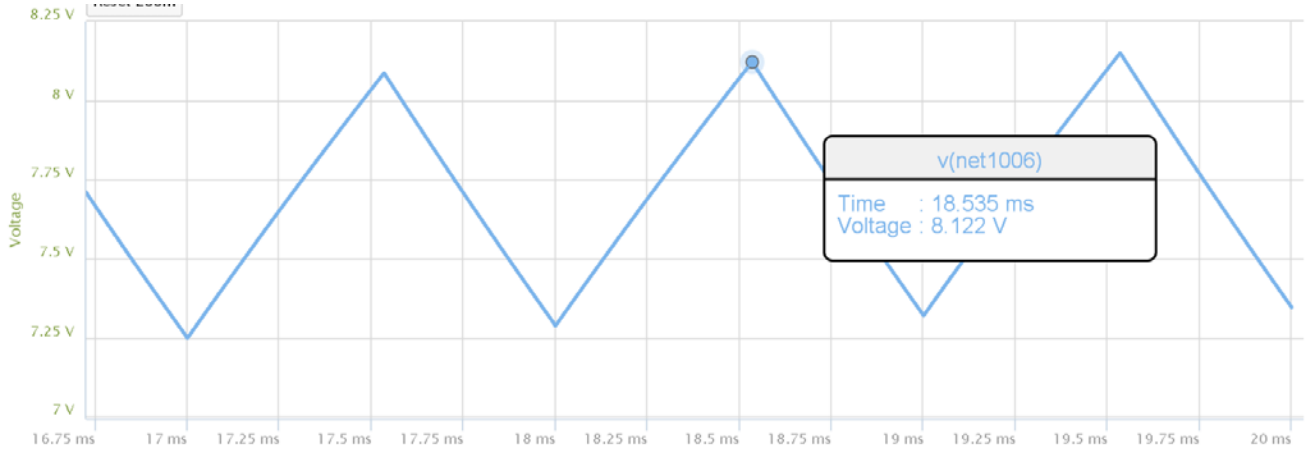
$$500mV_{pp} = \left(\frac{80}{80+j\omega L}\right) 15V_{pp}$$

$$|80 + j6280L| = 2400\Omega$$

$$L = 0.382H$$

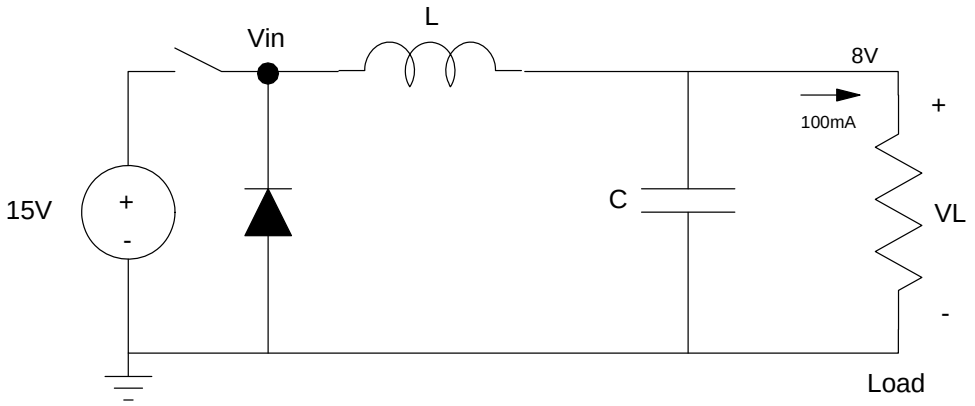


Buck Converter: Input modeled as a 15.7V pulse (15V plus 0.7V drop across D1) with a pulse width of 8/15 ms



Voltage at the load: 7.289V < Vout < 8.122V (833mVpp)

6) Modify your design for problem 5 to include a capacitor so that the ripple is reduced to 100mVpp with a load of 100mA.



Problem 5-6

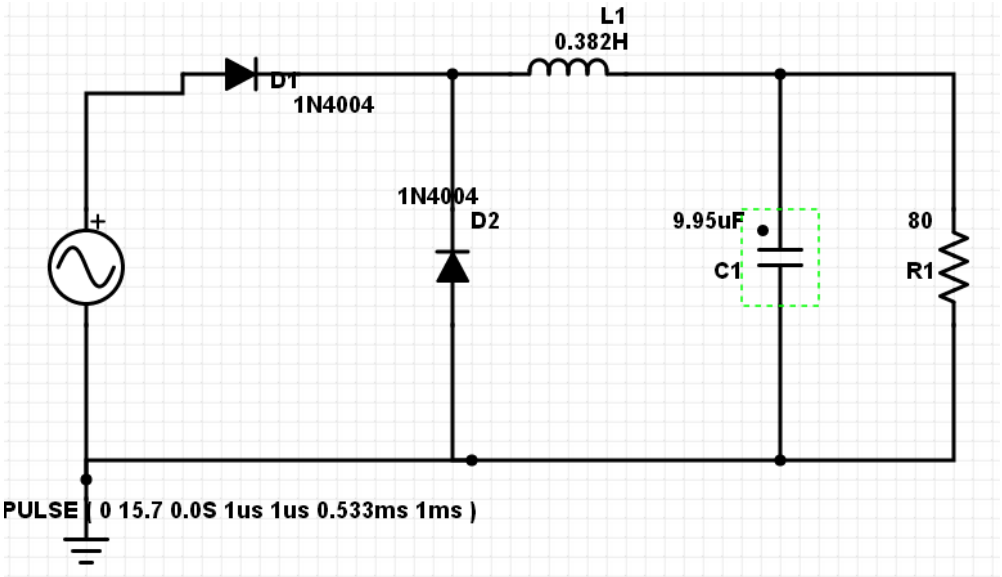
By voltage division

$$100mV_{pp} = \left(\frac{R||\frac{1}{j\omega C}}{R||\frac{1}{j\omega C}+j\omega L}\right)15V_{pp}$$

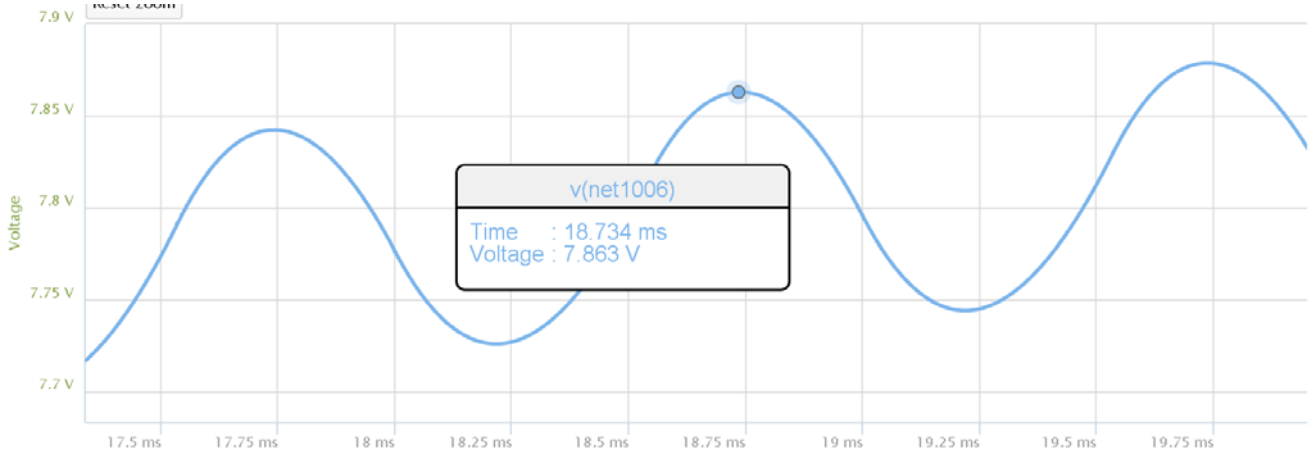
$$\omega^2 LC \approx \frac{15V_{pp}}{100mV_{pp}}$$

$$6280^2 \cdot 0.382H \cdot C \approx 150$$

$$C \approx 9.95\mu F$$



Buck Converter with LC selected for 100mVpp ripple



Resulting voltage at the output: 7.726V < Vout < 7.863V (137mVpp)

Lab:

7) Testing: Simulate one of these circuits in PartSim to test your analysis

8) Validation: Build one of these circuits in lab and verify the voltage and the ripple.