

ECE 320 - Quiz #7 - Name _____

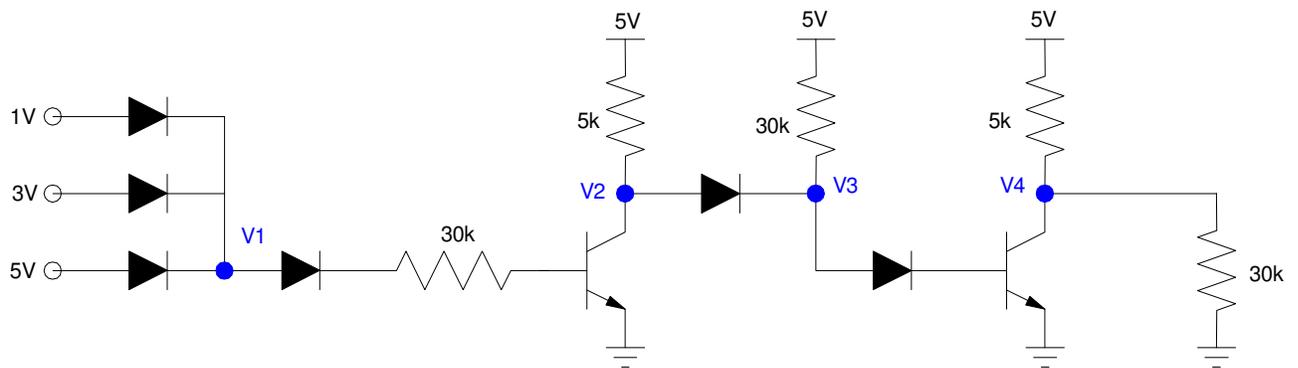
DTL Logic, TTL Logic, MOSFETs. March 12, 2020

1) Determine the voltages for the following DTL gate. Assume ideal silicon diodes ($V_f = 0.7V$) and transistors:

$V_{be} = 0.7V$

- $V_{ce(sat)} = 0.2V$
- $\beta = 100$

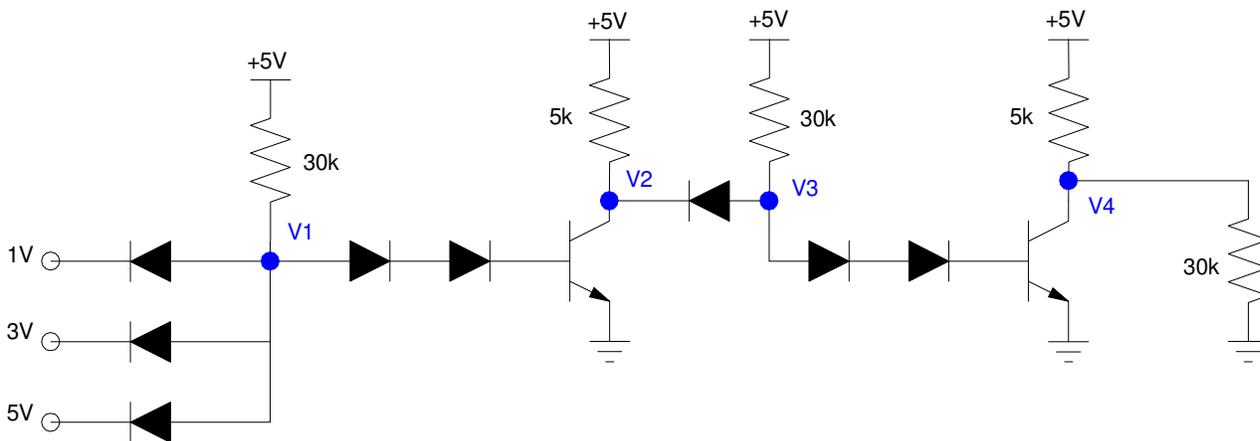
V1	V2	V3	V4



2) Determine the voltages for the following DTL gate. Assume ideal silicon diodes ($V_f = 0.7V$) and transistors:

- $V_{be} = 0.7V$
- $V_{ce(sat)} = 0.2V$
- $\beta = 100$

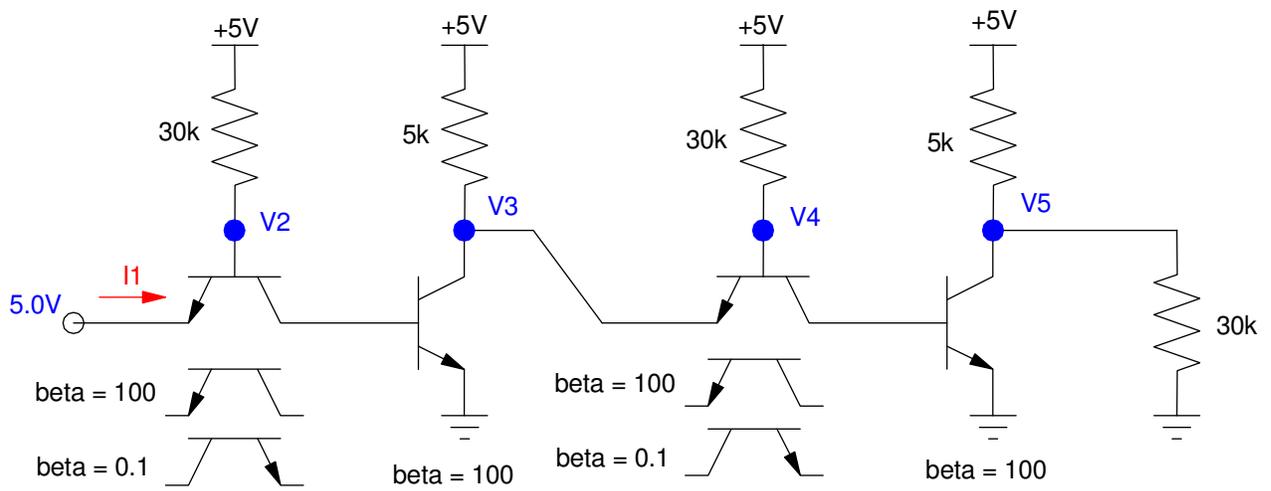
V1	V2	V3	V4



3) Determine the voltages for the following TTL gate. Assume ideal silicon diodes ($V_f = 0.7V$) and transistors:

- $V_{be} = 0.7V$
- $V_{ce(sat)} = 0.2V$
- $\beta = 100$ or 0.1

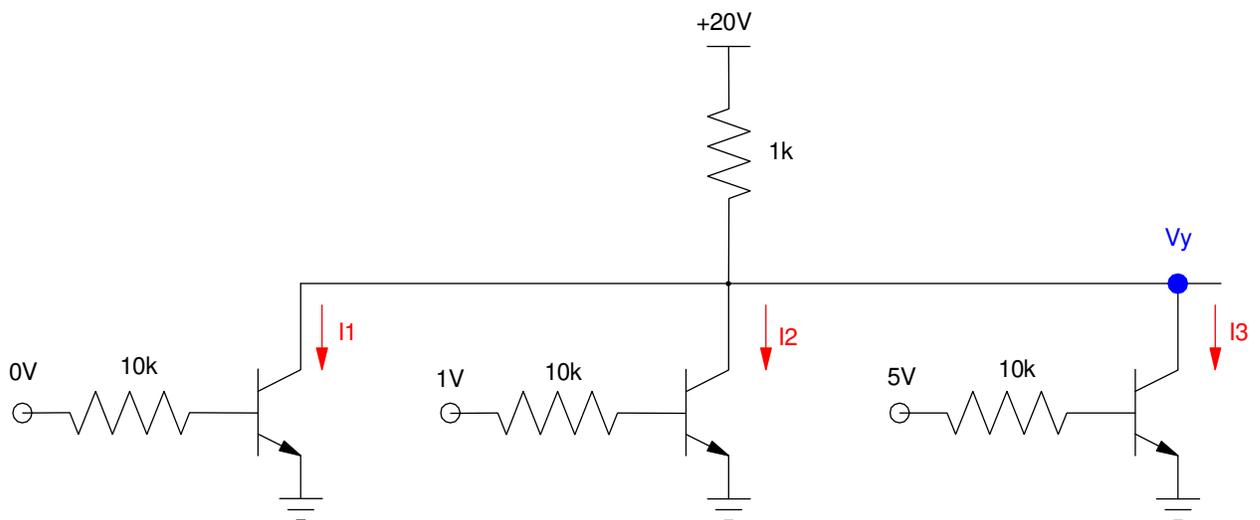
I1	V2	V3	V4	V5



4) Determine the voltages and currents for the following open-collector circuit. Assume ideal silicon diodes ($V_f = 0.7V$) and transistors:

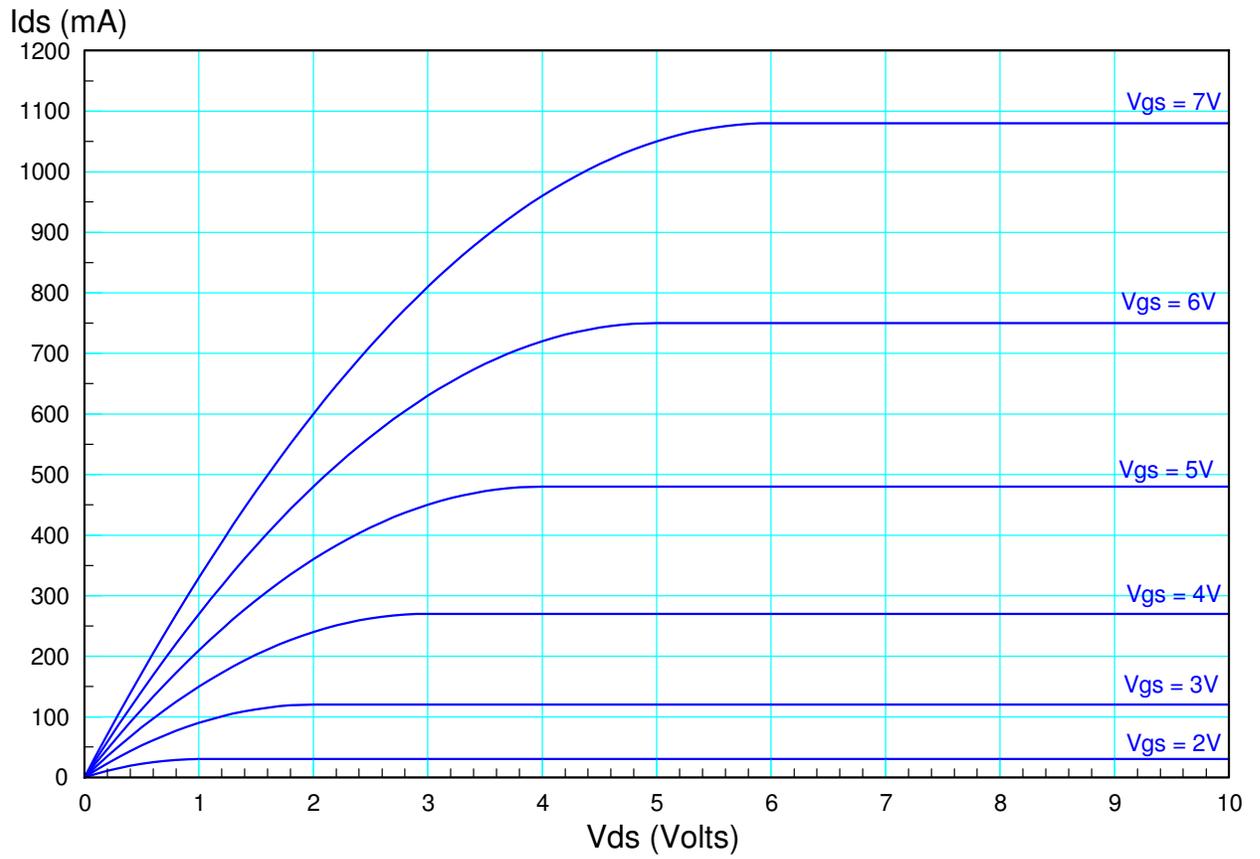
- $V_{be} = 0.7V$
- $V_{ce(sat)} = 0.2V$
- $\beta = 100$

I1	I2	I3	Vy



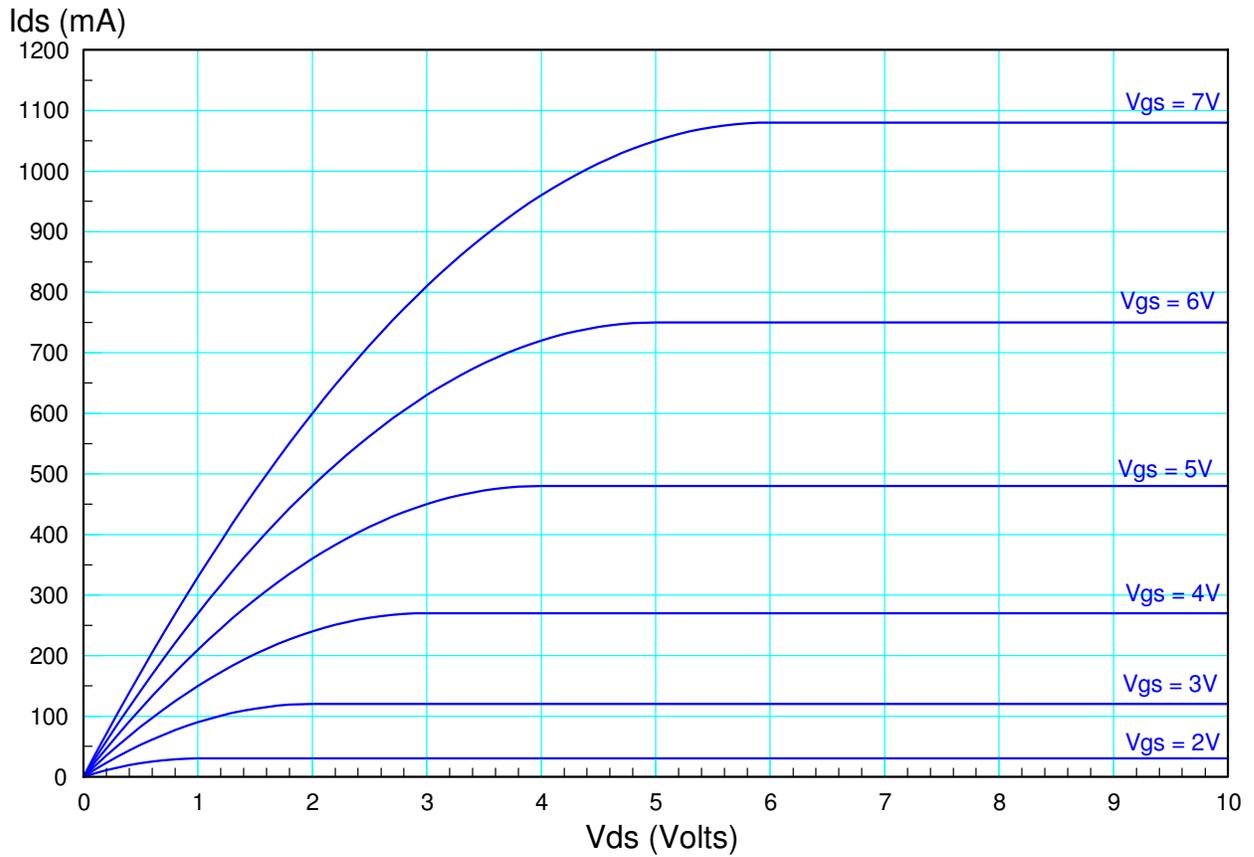
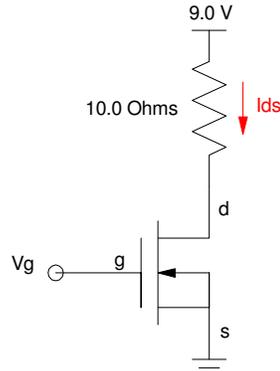
5) Determine k_n and label the off / saturated / ohmic regions for the following MOSFET.

k_n	Off Region	Ohmic Region	Saturated Region
	show on graph	show on graph	show on graph



6) Draw the load-line for the following circuit and determine the q-point (V_{ds} , I_{ds}) for $V_g = \{1V, 3V, 5V\}$

Load Line	$V_g = 2.0\text{ V}$	$V_g = 4.0\text{ V}$	$V_g = 6.0\text{ V}$
show on graph	$V_{ds} =$	$V_{ds} =$	$V_{ds} =$
	$I_{ds} =$	$I_{ds} =$	$I_{ds} =$



Bernie Sanders Bonus! According to the Las Vegas betting line, which is more likely to happen this year:

- The Vikings winning the Super Bowl,
- Bernie Sanders being elected President