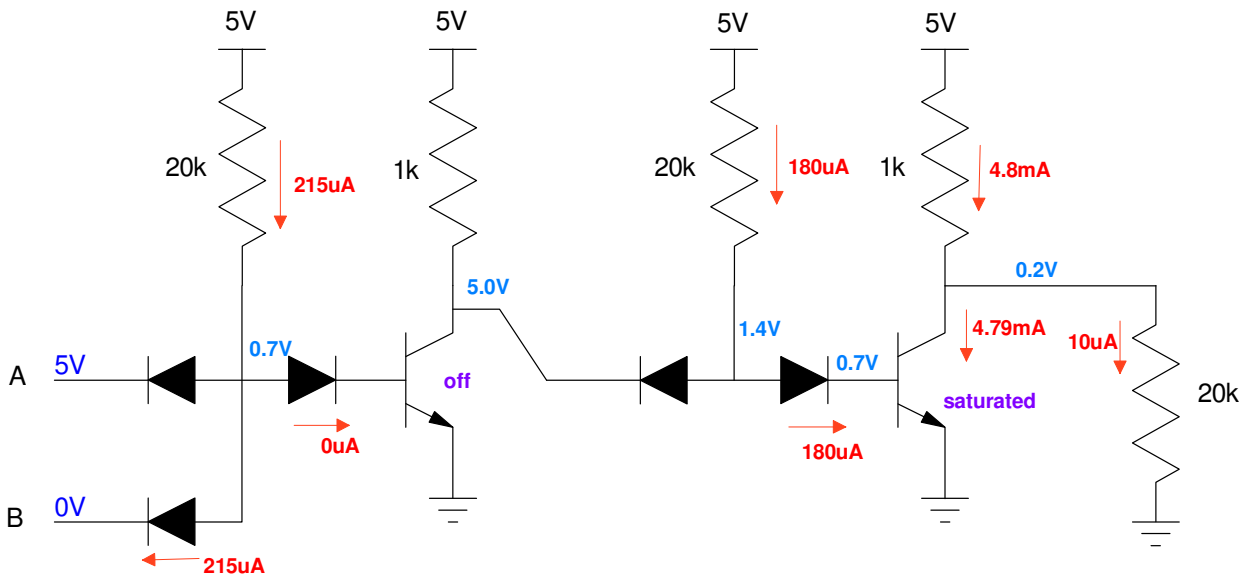
ECE 320 - Homework #8

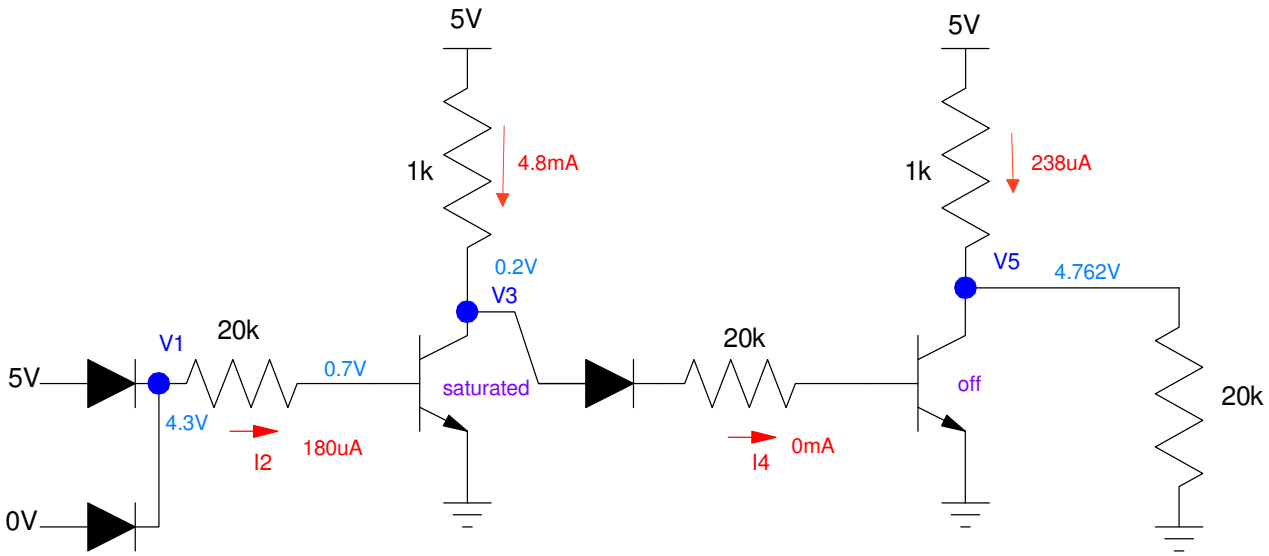
DTL, TTL Logic, MOSFETs. Due Monday, March 9th

DTL Logic

1) Determine the voltages and currents for the following DTL AND gate. Assume 3904 transistor (Vce = 0.2V, Vbe = 0.7V, β=100)

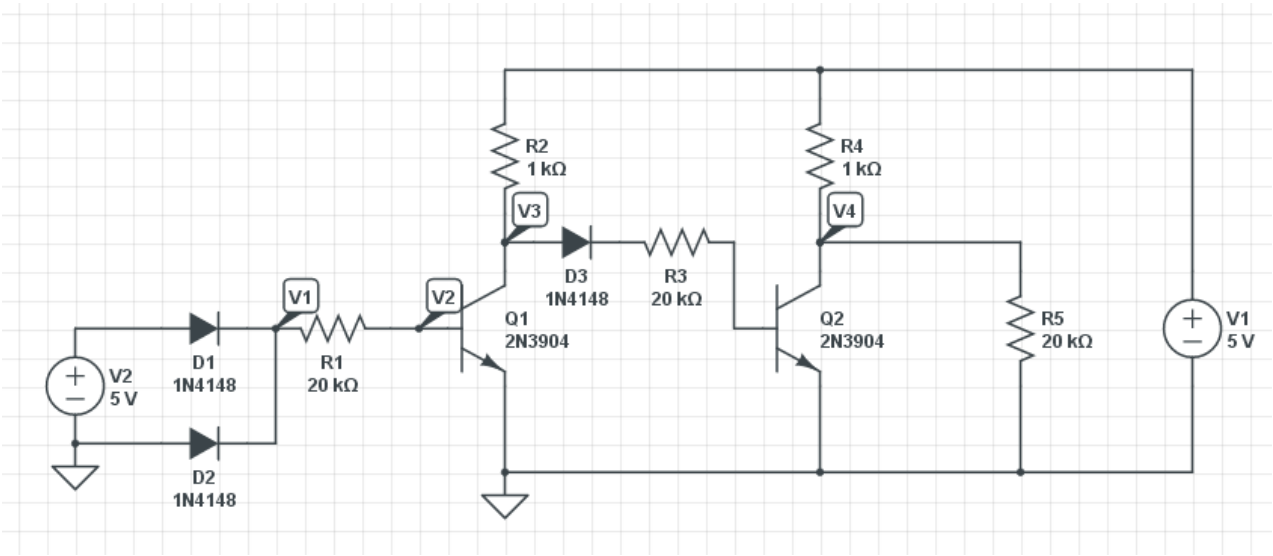


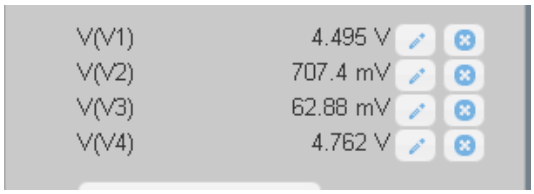
2) Determine the voltages and currents for the following DTL OR gate. Assume 3904 transistors



3) (Lab): Build a DTL NOR gate in lab. Measure

- The votlages when the input is { 0V, 0V },
- The votlages when the input is { 0V, 5V }, and
- The maximum frequency the logic gate can respond to (apply a square wave at the input)





	Calculated	Simulated (lab)
V1	4.30 V	4.495 V
V2	0.70 V	0.707 V
V3	0.20 V	0.063 V
V4	4.762 V	4.762 V

Results when Va = 5V, Vb = 0V

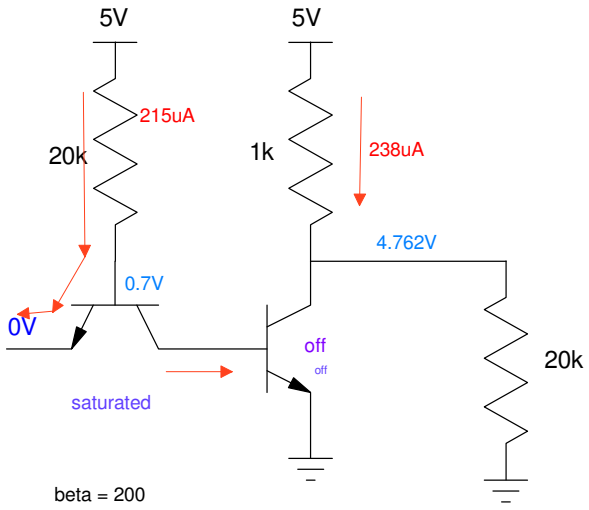
	Calculated	Simulated (lab)
V1	0 V	15nV
V2	0 V	15nV
V3	5.00 V	4.82 V
V4	0.20 V	0.064 V

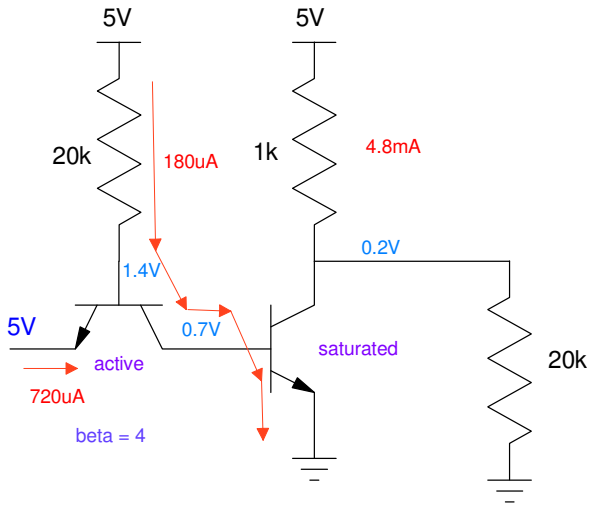
Results when Va = Vb = 0V

TTL Logic

4) Determine the voltages for the following TTL inverter. Assume 3904 transistors.

- $\beta = 200$ when used correctly
- $\beta = 4$ when used backwards (found in lab)

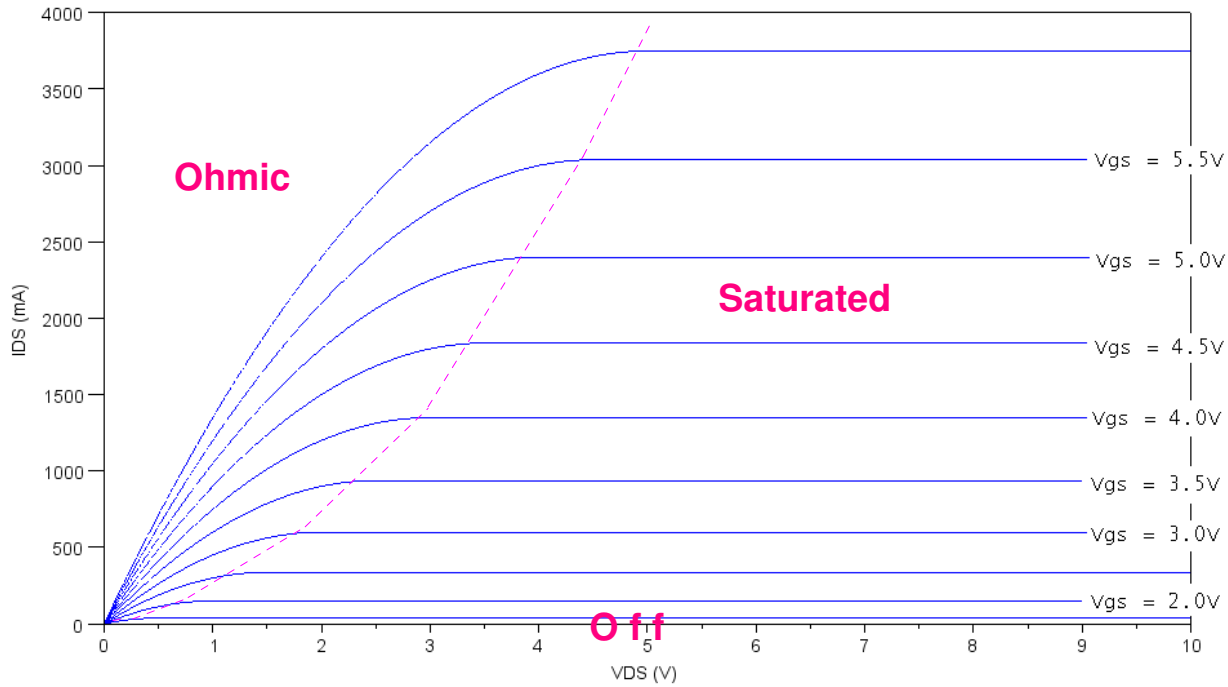




MOSFET

5) The VI characteristics for an n-channel MOSFET is shown below. Assume Vth = 1.0V

- Determine the transconductance gain, kn
- Label the off / saturated / ohmic regions in the curve below.



To calculate the transconductance gain, pick a point

Vds = 8V, Ids = 3.8A, Vgs = 6.0V

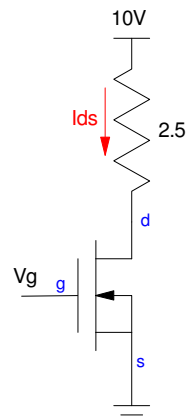
This is in the saturated region

$$I_{ds} = \frac{k_n}{2}(V_{gs} - V_{th})^2$$

$$3.8A = \frac{k_n}{2}(6-1)^2$$

$$k_n = 0.304\ \frac{A}{V^2}$$

6) Draw the load line and mark the operating points for Vg = { 0V, 5V, 7V }



0V: Off region

Ids = 0, Vds = 10V

5V: Saturated Region

$$I_{ds} = \frac{0.304}{2}(5-1)^2 = 2.432A$$

$$V_{ds} = 10 - 2.5I_{ds} = 3.92V$$

7V: Ohmic Region

$$I_{ds} = 0.304\left(7 - 1 - \frac{V_{ds}}{2}\right)V_{ds}$$

$$V_{ds} + 2.5I_{ds} = 10$$

Solving

Ids = 3.16A, Vds = 2.109V