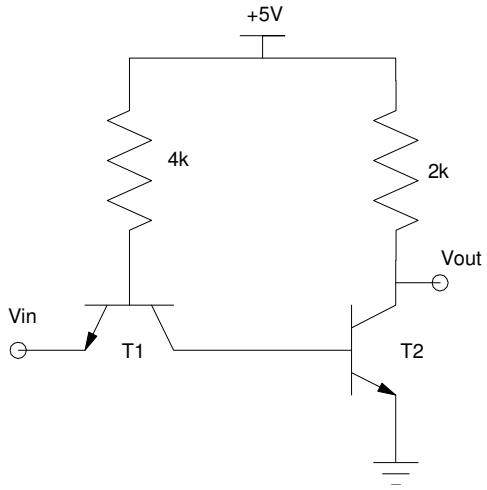
Transistor Transistor Logic (TTL)

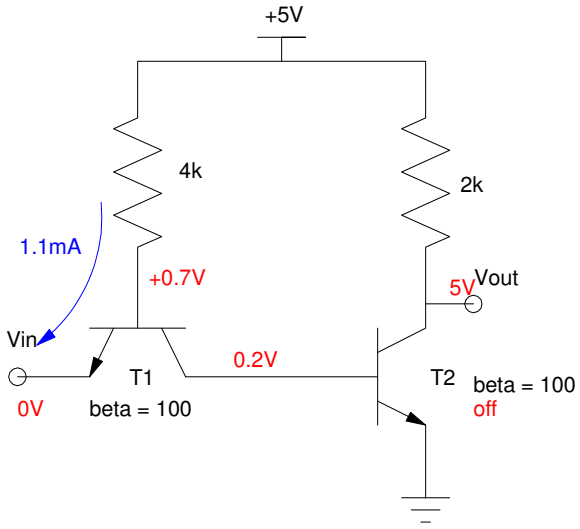
An improved form of digital logic uses two transistors rather than a diode, and is termed Transistor Transistor Logic (TTL). The basic circuit for a TTL inverter is as follows:



First, let's look at what happens when Vin = 0V. In this case, transistor T1 saturates: the +5V supply sees a path to ground through the 4k resistor, the diode in T1, to ground. This turns on T1, saturating it. (No current flows from the base of T2, so you satisfy the saturated condition:

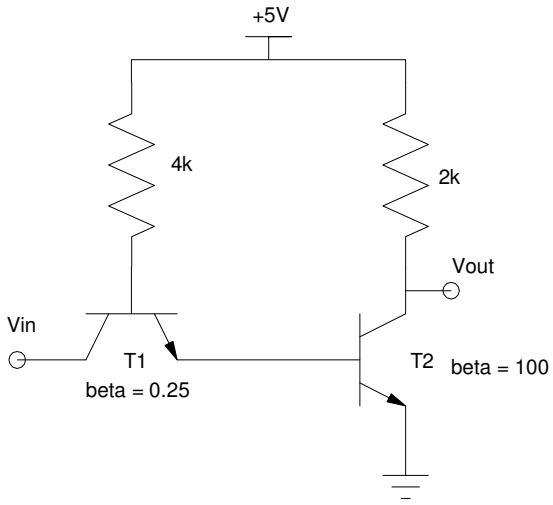
$$\beta I_{BE} > I_{CE} = 0$$

For transistor 2, you don't have enough voltage to force current to flow in it's diode, so T2 turns off. This results in Vout being pulled to +5V through a 2k resistor.

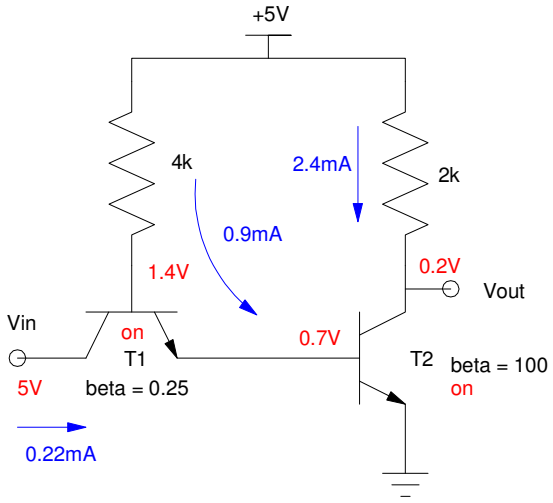


Next let's look at what happens with Vin = +5V. This circuit is a little confusing since now T1 is actually placed in the circuit backwards. If you take an NPN transistor and reverse the leads, you wind up with an NPN transistor. Hence, putting it in a circuit backwards still results in an NPN transistor.

The doping is all wrong, however, so instead of getting a gain of 300, you get a gain of something like 0.25. So, let's redraw the circuit with the transistor draws the way it's used - just recall that the gain is really bad (0.2).



Using this circuit with Vin = +5V results in



Note that you have an inverter:

Vin = 0V	Vout = 5V
Vin = 5V	Vout = 0.2V

Power: The power dissipated in this inverter is

Vin = 0V:

I = 1.1mA

$$P = VI = (5V)(1.1mA) = 5.5mW$$

Vin = 5V:

I = 0.9mA + 2.4mA = 3.3mA

$$P = VI = (5V)(3.3mA) = 16.5mW$$

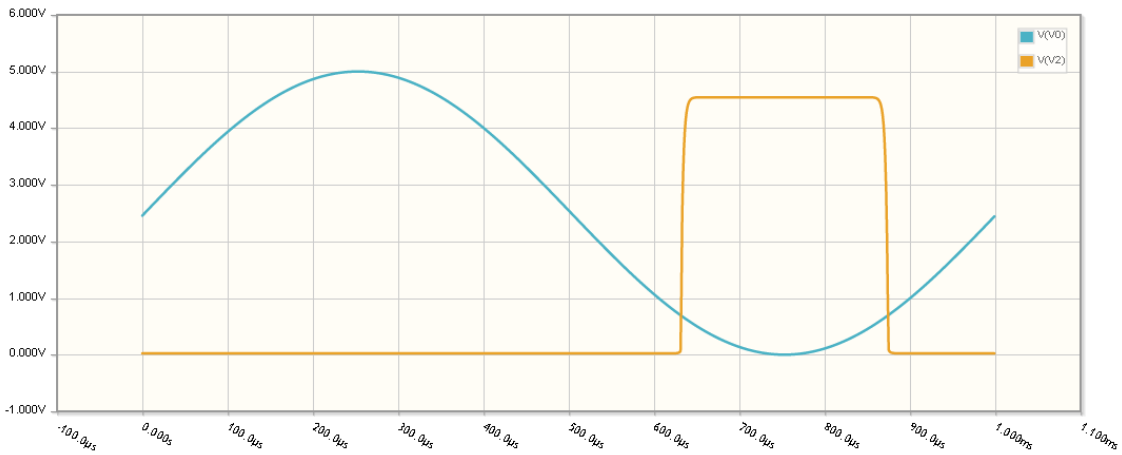
Logic Levels: To turn on T1, Vin > 0.9V: (Vb for T2 is 0.7V. Vce for T1 is about 0.2V. Vin needs to be at least 0.7V + 0.2V).

- Logic Level 0 is a voltage less than 0.9V.

Logic level 1 is a voltage slightly higher than this.

In CircuitLab, you can test this by sweeping the input voltage and noting when the output is logic level 1 or 0.

- Vin > 700mV Transistor is saturated (Logic level 1 is more than 700mV)
- Vin < 522mV Transistor is off (Logic level 0 is less than 522mV)



Fanout: You can only drive a limited number of gates with a single inverter. Assume, for example, a single inverter whose output is 5V tries to drive a load of N inverters.

- Each load draws 0.22mA at 5V.
- This 0.22mA passes through the 2k resistor at the output of the first inverter.
- This drops the output voltage by V = IR.
- If you can only allow a 4V drop (Vout of the first stage is 4V), you can only drive

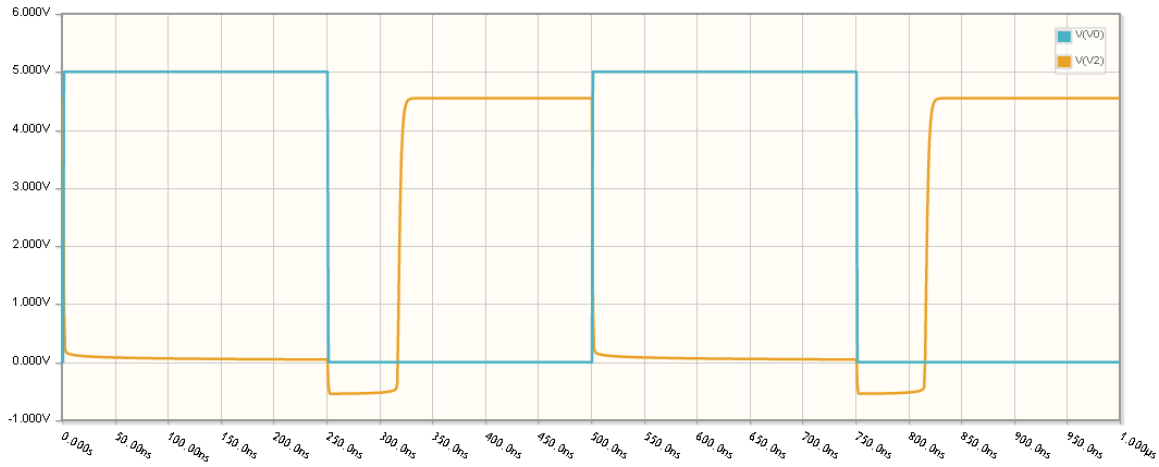
$$V_{drop} = 4V = N \cdot (2k\Omega)(0.22mA/load)$$

N = 9

A single NOT gate can only drive nine gates. This is termed the fanout limit.

Max Clock Frequency

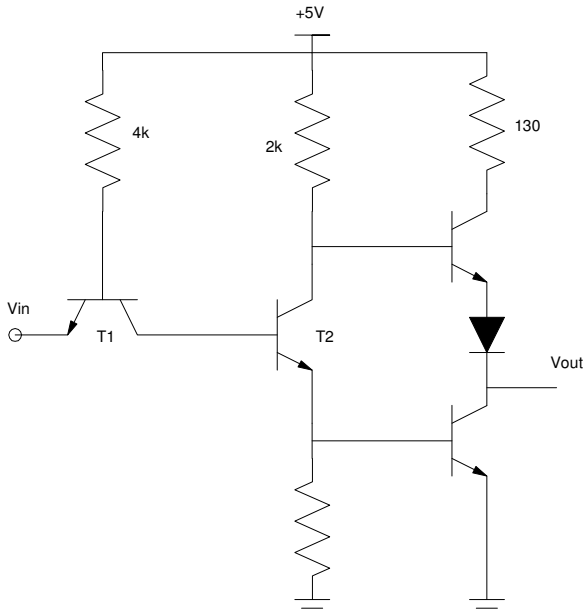
It takes about 80ns for the output to go from logic level 0 to level 1. This limits the maximum clock frequency to about 10MHz.



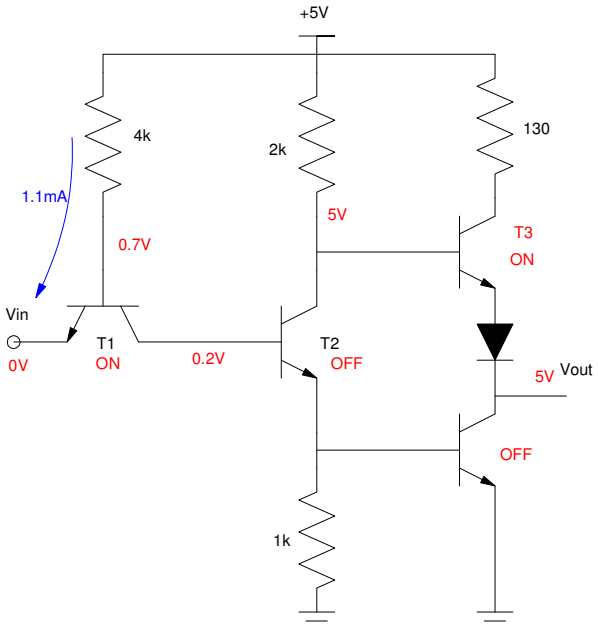
CircuitLab simulation of a TTL inverter with 2MHz input.

7400 Series of TTL Inverters

The previous TTL inverter is the heart of the 7400 series inverters.



First, let's assume Vin = 0V.



The 5V supply sees a path to ground through the 4k resistor and the diode in T1. This saturates transistor T1, pulling the base voltage of T2 to 0.2V. This turns off T2, raising the collector voltage to +5V. This turns on T3, which pulls the output up to +5V (with no load). If you have a load, such as a 10k resistor at the load, the output is pulled up to

$$V_{out} = 5V - 130\Omega \cdot I_{c3} - 0.7V$$

$$V_{out} = 5V - 130\Omega \cdot \left(\frac{5V - 0.7V}{10k\Omega + 130\Omega}\right) - 0.7V$$

$$V_{out} = 4.24V$$

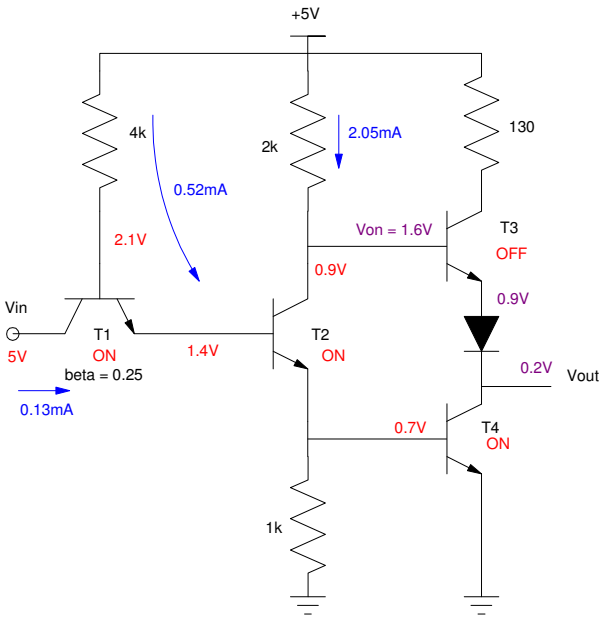
It's at logic level 1. The NOT gate consumes

$$P = (5V)(1.1mA) = 5.5mW$$

Further, transistor T2 remains off as long as you don't have enough voltage to saturate T1 (0.2V) plus turn on the diode in T2 (0.7V) plus turn on the diode in T4 (0.7V).

$$\text{Logic } 0 = V_{in} < 0.2V + 0.7V + 0.7V = 1.6V$$

Next, let's see what happens when Vin = +5V. Again, I'll redraw T1 so it is flipped - resulting in a current gain of 0.25.



If Vin = +5V:

- The +5V supply sees a path to ground through the 4k resistor, through diode T1, diode T2, and diode T4. This turns on and saturates transistors T1, T2, and T4.
- With T4 saturated, the output is 0.2V.
- With the output diode, the emitter of T3 is 0.9V.
- The base of transistor T3 needs to be 0.7V above the emitter to turn on (1.6V). However, since T2 is saturated, the base of T3 is only 0.9V. This turns off transistor T3.

The net results is the output is logic 0 (0.2V). It remains at 0.2V as long as the input is above 1.6V.

The transition from logic 0 to logic 1 for TTL logic is 1.6V

Power Consumption:

$$P = 5V(0.52mA + 2.05mA) = 12.8mW$$

Fanout:

If an inverter whose output is logic 1 tries to drive N inverters, the output must remain above 1.6V to be read as logic 1.

$$V_{out} > 1.6V$$

But

$$V_{out} = 5V - 130\Omega \cdot I - 0.7V > 1.6V$$

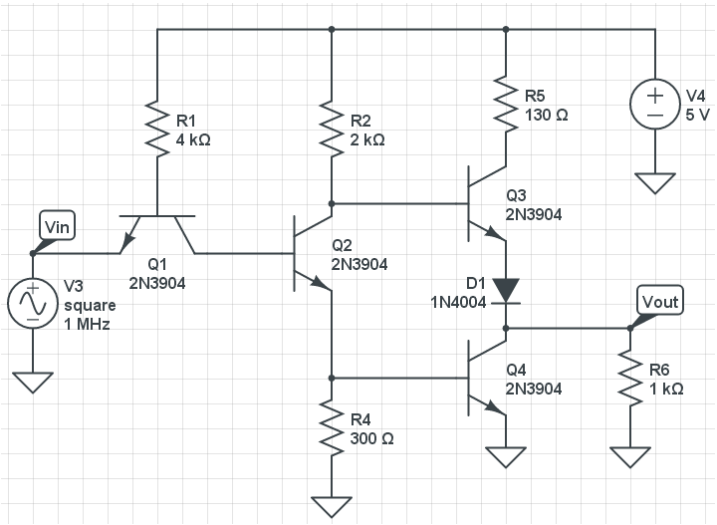
Each load draws 0.13mA, so

$$5V - 130\Omega \cdot (N \cdot 0.13mA) - 0.7V > 1.6V$$

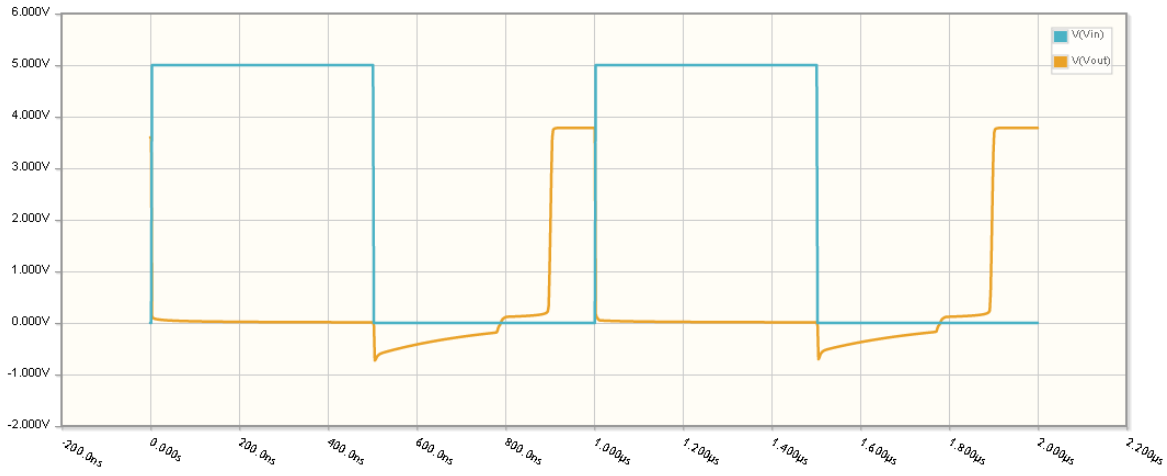
$$N < 159$$

A single inverter can drive 159 inverters (the fanout is 159). That's a lot better than what we had before, and is the purpose of the additional two transistors at the output stage. Typical fanouts are listed as being only 10, however, in the data sheets. This is somewhat conservative to account for variations in gain, resistance, etc.

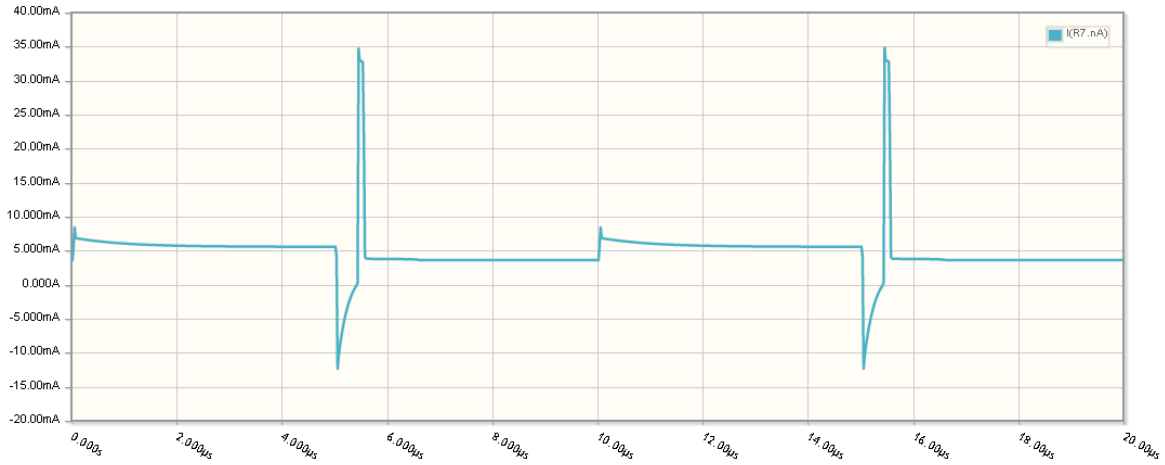
CircuitLab Simulation



7400 TTL inverter for CircuitLab



It takes about 400ns to go from logic level 0 to level 1, limiting the clock speed to 2MHz



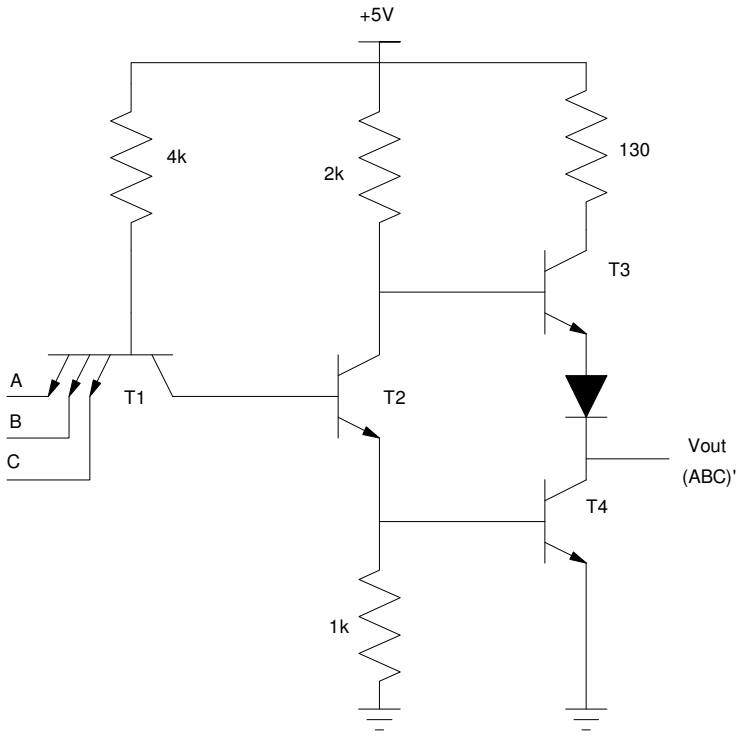
Current Consumption for TTL Logic. Spikes appear on the current line whenever you have a 1 / 0 transition

TTL NAND gate:

To build a TTL NAND gate, transistor T1 is built so that the base has several inputs. The diode from the pn junction results in the net effect being the minimum voltage of A, B, and C determining how transistor T1 behaves. min(A,B,C) is the same as an AND function. Hence, this is an AND gate. Inverted - making it a NAND.

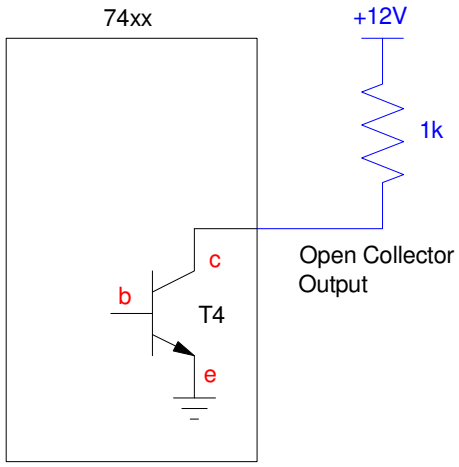
Note that it takes 4 transistors to build a NOT gate and 4 transistors to build a NAND gate.

- You don't gain anything by replacing NAND gates with a single input with an inverter
- To determine the number of transistors in your design, multiply the number of NAND and NOT gates by 4.



Open Collector Outputs:

The 7400 series of TTL gates have several which are open-collector outputs. In essence, T3 and the 130 Ohm resistor are removed, leaving the output connected only to T4.



Output for a 74xx chip with open-collector output

Open collector outputs have an output which is

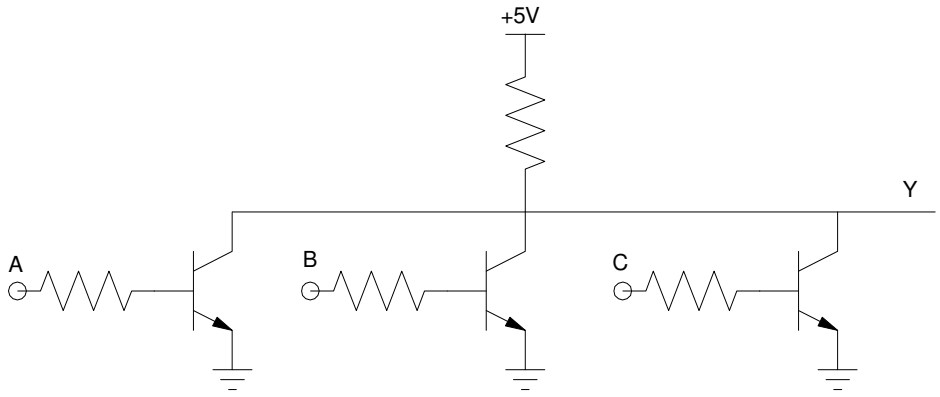
- floating if logic 1 (transistor T4 is off)
- grounded if logic 0 (transistor T4 is saturated).

To convert this to an output, you need a pull-up resistor connected to the output.

What this buys you is...

- You don't have to have 5V output. Simply pull the output up with a 1k resistor and a +12V source and the output is 0V (logic 0) and +12V (logic 1).
- You can use wired-or logic. Connect N open-collector outputs together (short them) and use a single pull-up resistor. If any of them are logic 0, the output is grounded (logic 0). The output is only logic 1 if all the outputs are logic 1. You get a NOR gate for free - just connect the outputs together.

Wired or logic is nice since it avoids conflicts. If one output says logic 0 and another says logic 1, you don't blow any fuses, currents don't shoot to infinity, or any other problems. You just have the output grounded (logic 0) and floating (logic 1). Logic 0 wins.



Wired-OR logic. Y = 0 if A or B or C is 5V