TTL logic is used widely, but has a few limitations:

- The input impedance is not infinity. This limits the fanout.
- The corresponding power consumption is somewhat high (5mW computed previously).

To get around these problems, add a MOSFET to the input stage. The input impedance then becomes infinite (in theory). At the output, use a push-pull amplifier from before to provide some power at the output:

First, let's assume \( \text{Vin} = +5\text{V} \). This creates an n-channel in \( M1 \), turning it on. This shorts the base of the transistors to ground. The diode in \( T3 \) then pulls \( \text{Vout} \) to 0.7V (logic level 0).

The MOSFET \( M2 \) is turned off. p-channel MOSFETs are opposite of n-channel MOSFETs.

- \( \text{VGS} > \text{VT} \) to create an n-channel and turn on an n-channel MOSFET
- \( \text{VGS} < -\text{VT} \) to create a p-channel and turn on a p-channel MOSFET.

Since \( \text{Vin} = \text{Vg} = +5\text{V} \) in this case, you have \( \text{VG} > \text{VG} \) and the p-channel is not created. MOSFET \( M2 \) is off.

Next, let's assume \( \text{Vin} = 0\text{V} \).

- This turns off \( M1 \) (\( \text{VGS1} = 0\text{V} < \text{VTN} \)).
- This turns on \( M2 \) (\( \text{VS2} = 5\text{V}, \text{VGS2} = -5\text{V} < -\text{VTN} \)).

This pulls the base of the two transistors up to +5V. The diode in \( T4 \) then pulls the output up to 4.3V (logic 1).

Hence, you have an inverter:
- 0V in produces 4.3V out (logic level 1)
- 5V in produces 0.7V out (logic level 0).

The transition from logic level 0 to 1 is determined by VTN for the MOSFETs.  

Note that there isn't a problem with cascading these inverters. The input current is zero. Hence, you can add as many as you like (in theory) to the output. Further, the power consumption is also zero (in theory). One of the transistors is always off, meaning no current flow through them. One MOSFET is always off as well, meaning no current flow through that path. The only time you consume power is when you change states.

The only problem is you lose 0.7V at each stage. You can add a stage at the output to bring this back up to +5V.

**CMOS Logic Gates**

You can also create logic gates with CMOS by using them as a switch. For example, if you use the switch we had before with several n-channel MOSFET's in parallel as shown on the left below, the output is low if any of the inputs, A, B, or C, is +5V. This creates a NOR gate

\[
\bar{Y} = A + B + C \\
Y = (A + B + C)' \quad \text{(NOR)}
\]

If you flip the resistor and the MOSFET's, and use p-channel MOSFETs as shown on the right, the output is pulled high if A, B, or C is 0V (turning on the p-channel MOSFET). This creates a NAND gate.

\[
Y = \overline{A + B + C} \\
\bar{Y} = \left( \overline{A + B + C} \right) = ABC
\]
You can also place the MOSFET's in series. If you place the MOSFET's on the low side as shown on the left, the output is pulled low only if all three MOSFETs are turned on (A, B, and C are all 5V). This creates a NAND gate.

\[
\bar{Y} = ABC \\
Y = \overline{ABC} \quad \text{(NAND)}
\]

If you place the MOSFET's on the high side and use p-channel MOSFETs, the output is high only if A, B, and C are 0V (turning on the three MOSFETs): you have a NOR gate.

\[
Y = \overline{A \cdot B \cdot C} \\
Y = \overline{(A + B + C)} \quad \text{(NOR)}
\]

The problem with these designs is they waste power: when the MOSFET's are turned on, you are dumping current in the resistor. A more efficient design is to combine the above circuits so that the output is either pulled high (with the MOSFETs to ground turned off) or pulled low (with the MOSFETs to power turned off.)

Combining the above circuits results in the following improved NAND and NOR gates:
Improved 3-input NAND gate (left) and NOR gate (right)

One thing you might notice with this design is when switching from logic 0 to 1 or visa versa, there is a chance that the MOSFET's to +5V will remain on for a brief time while the MOSFET's to ground turn on. This results in power being shorted to ground for a brief moment. In the lab, if you look at the power signal, you can sometimes see spikes on the power line whenever a gate switches logic levels.