## ECE 376 - Test \#1: Name

Spring 2023

1) Digital Inputs. Design a circuit which outputs

- 0 V when $\mathrm{R}<1500$ Ohms
- 5 V when $\mathrm{R}>1700 \mathrm{Ohms}$

Assume

- R1 $=800+100^{*}$ (your birth month) + (your birth date).
- May 14th, for example, gives R1 = 1314 Ohms

$\mathrm{R}=1500$ (off)

$$
V_{a}=\left(\frac{1500}{1500+1314}\right) 5 V=2.6652 V
$$

$\mathrm{R}=1700$ (On)

$$
V_{a}=\left(\frac{1700}{1700+1314}\right) 5 V=2.8202 V
$$

$\mathrm{V}(\mathrm{on})>\mathrm{V}($ off $)$ so connect to the plus input
Output turns on at 2.82 V - make the offset 2.82 V

$$
\text { gain }=\left(\frac{5 V-0 V}{2.8202 V-2.6652 V}\right)=32.27
$$

2) Digital Outputs: Design a circuit which allows your PIC to drive a 100W LED at N mA

- $\mathrm{N}=800+100^{*}$ (your birth month) + (your birth date)
- $\mathrm{N}=1314 \mathrm{~mA}$ for May 14th, for example

Assume a 20W LED has the following characteristics

- $\mathrm{Vf}=10 \mathrm{~V} @ 2000 \mathrm{~mA}$
- 2,000 Lumens @ 2000mA

Assume a 6144 NPN transistor

- $\mathrm{Vbe}=700 \mathrm{mV}$
- Vce(sat) $=360 \mathrm{mV}$
- Current gain $=\beta=200$

| Ic $(\mathrm{mA})$ <br> $800+100^{*}$ Month + Day | Lumens <br> Light output when on | Rb | Rc |
| :---: | :---: | :---: | :---: |
| 1314 mA | 1314 | $172 . .654$ | $\mathbf{7 . 3 3}$ |

$$
\begin{aligned}
& \text { Light }=\left(\frac{1314 \mathrm{~mA}}{2000 \mathrm{~mA}}\right) 2000 \text { Lumens }=1314 \text { Lumens } \\
& R_{c}=\left(\frac{20 \mathrm{~V}-10.36 \mathrm{~V}}{1314 \mathrm{~mA}}\right)=7.33 \Omega
\end{aligned}
$$

Range of Rb

$$
\begin{aligned}
& \min \left(I_{b}\right)=\left(\frac{I_{c}}{\beta}\right)=\left(\frac{1314 m A}{200}\right)=6.57 m A \\
& R_{b}=\left(\frac{5 V-0.7 V}{6.57 \mathrm{~mA}}\right)=654 \Omega
\end{aligned}
$$



$$
\begin{aligned}
& \max \left(I_{b}\right)=25 m A \\
& R_{b}=\left(\frac{5 V-0.7 V}{25 m A}\right)=172 \Omega
\end{aligned}
$$

3) Assembler: Determine the contents of the W , A , and B after each operation. Assume - A and B are 8 -bit registers (spots in memory).

- Default is decimal

|  | W | A | B |
| :---: | :---: | :---: | :---: |
| Start: | 13 | Birth Month (1..12) $5$ | Birth Date (1..31) 14 |
| incf A, W | 6 | 5 | 14 |
| decf B,W | 13 | 5 | 14 |
| addlw 5 | 18 | 5 | 14 |
| addwf A, F | 18 | 23 | 14 |
| subwf B,W | $252$ <br> -4 is also correct | 23 | 14 |
| movf A,W | 23 | 23 | 14 |
| movff A, B | 23 | 23 | 23 |
| andlw 7 | 7 | $\begin{gathered} 23 \\ 00010111 \end{gathered}$ | 23 |
| btg A, 1 | 7 | 21 <br> 00010101 | 23 |
| movwf B | 7 | 21 | 7 |

## 4) Assembler \& Timing:

a) Determine the number of clocks the following assembler subroutine takes to execute.

- Assume MONTH and DAY be your birth month and day.
b) Modify this routine (change A, B, and C) so that it takes $2,500,000$ clocks ( 250 ms ) to execute
- +/- 50,000 clocks
\(\left.$$
\begin{array}{|c|c|c|c|}\hline \text { A } & \begin{array}{c}\text { Month } \\
\text { birth month } 1.12\end{array} & \begin{array}{c}\text { Day } \\
\text { birth date } 1 . .31\end{array} & \begin{array}{c}\mathrm{N} \\
\text { number of clocks Wait takes }\end{array}
$$ <br>
\hline 150 \& \mathbf{5} \& \mathbf{1 4} \& \mathbf{6 7 , 8 0 8} <br>

6 \mathrm{ABC}+5 \mathrm{AB}+7 \mathrm{~A}+8\end{array}\right]\)| N |
| :---: |
| A |

Other values also work.
Limitations: A, B, C are all integers, in the range of $1 . .255$

```
Wait:
    movlw 150 (A)
    movwf CNT2
    nop
    nop
    nop
    nop
W2:
\begin{tabular}{ll} 
movlw & MONTH \\
movwf & CNT1 \\
nop & \\
nop &
\end{tabular}
(B)
W1:
movlw DAY (C)
movwf CNT0
W0:
```

```
nop
```

nop
nop
nop
nop
nop
decfsz CNT0,F
decfsz CNT0,F
goto W0
goto W0
decfsz CNT1,F
goto W1

```
decfsz CNT2,F
goto W2
5) Assember \& Flow Charts. Write an assembler program to turn your PIC processor into random count-down timer
- When RB0 is pressed, PORTC counts from \(1 . .12\) really fast
- When RB0 is released, PORTC then contains a random number from \(1 . .12\)
- PORTC then counts down every 250 ms
- When PORTC reaches zero, it then goes back to the beginning and waits for RB0.

Assume a 250 ms wait routine exists (call Wait)
```

    org 0x800
    movlw 0x0F
    movwf ADCON1
    movlw 0xFF
    movwf TRISB
    clrf TRISC
    btfss PORTB,0
    goto L1
    btfss PORTB,0
    goto L6
    incf PORTC,F
    movlw 12
    cpfsgt PORTC
    goto L5
    goto L2
    movlw 1
    movwf PORTC
    goto L2
    call Wait
    decf PORTC,F
    movlw 0
    cpfseq PORTC
    goto L6
    goto L1
    ```
L1:
L2:
L3:
L4:
L5:
L6:
L7:


Bonus: (Due Monday 2pm): Program and demonstrate problem \#5 on yor PIC board
\begin{tabular}{|c|c|c|c|}
\hline \multicolumn{4}{|l|}{Memory Read \& Write} \\
\hline MOVWF & PORTA & memory write & w g PORTA \\
\hline MOVFF & PORTA PORTB & copy & PORTA g PORTB \\
\hline MOVF & PORTA, W & memory read & PORTA g W \\
\hline MOVLW & 234 & Move Literal to WREG & 123 g W \\
\hline \multicolumn{4}{|l|}{Memory Clear, Negation} \\
\hline CLRF & PORTA & clear memory & \(0 \times 00 \mathrm{~g} \mathrm{PORTA}\) \\
\hline COMF & PORTA, W & toggle bits & !PORTA g W (bit toggle) \\
\hline NEGF & PORTA, W & negate & -PORTA g W (2's compliment) \\
\hline \multicolumn{4}{|l|}{Addition \& Subtraction} \\
\hline INCF & PORTA, F & increment & PORTA + 1 g PORTA \\
\hline ADDWF & PORTA, F & add & PORTA + W g PORTA \\
\hline ADDWFC & PORTA, W & add with carry & PORTA + W + carry g W \\
\hline \multicolumn{2}{|l|}{ADDLW} & Add Literal and WREG & \\
\hline DECF & PORTA, F & decrement & PORTA -1 g PORTA \\
\hline SUBFWB & PORTA, F & subtract with borrow & PORTA - W - c g PORTA \\
\hline SUBWF & PORTA, F & subtract no borrow & PORTA - W g PORTA \\
\hline SUBWFB & PORTA, F & subtract with borrow & PORTA - W - c g PORTA \\
\hline SUBLW & 223 & Subtract WREG from \# & 223-W g W \\
\hline \multicolumn{4}{|l|}{Shift left (*2), shift right (/2)} \\
\hline RLCF & PORTA, F & \multicolumn{2}{|l|}{rotate left through carry (9-bit rotate)} \\
\hline RLNCF & PORTA, F & \multicolumn{2}{|l|}{rotate left no carry} \\
\hline RRCF & PORTA, F & \multicolumn{2}{|l|}{rotate right through carry} \\
\hline RRNCF & PORTA, F & \multicolumn{2}{|l|}{rotate right no carry} \\
\hline \multicolumn{4}{|l|}{Bit Operations} \\
\hline \multicolumn{2}{|l|}{BCF PORTA, 3} & Bit Clear f & clear bit 3 of PORTA \\
\hline \multicolumn{2}{|l|}{BSF PORTA, 4} & Bit Set f & set bit 4 of PORTA \\
\hline \multicolumn{2}{|l|}{BTG PORTA, 2} & Bit Toggle f & toggle bit 2 of PORTA \\
\hline \multicolumn{4}{|l|}{Logical Operations} \\
\hline ANDWF & PORTA, F & logical and & PORTA \(=\) PORTA and W \\
\hline ANDLW & 0×23 & AND Literal with WREG & W = W and 0x23 \\
\hline IORWF & PORTA, F & logical or & PORTA = PORTA or W \\
\hline IORLW & 0x23 & Inclusive OR Literal & W = W or \(0 \times 23\) \\
\hline XORWF & PORTA, F & logical exclusive or & PORTA \(=\) PORTA xor W \\
\hline XORLW & 0x23 & Exclusive OR Literal & W = W xor \(0 \times 23\) \\
\hline \multicolumn{4}{|l|}{Tests (skip the next instruction if...)} \\
\hline CPFSEQ & PORTA & \multicolumn{2}{|l|}{Compare PORTA to W , skip if PORTA \(=\mathrm{W}\)} \\
\hline CPFSGT & PORTA & \multicolumn{2}{|l|}{Compare PORTA to W, Skip if PORTA > W} \\
\hline CPFSLT & PORTA & \multicolumn{2}{|l|}{Compare PORTA to W, Skip if PORTA < W} \\
\hline DECFSZ & PORTA, F & \multicolumn{2}{|l|}{decrement, skip if zero} \\
\hline DCFSNZ & PORTA, F & \multicolumn{2}{|l|}{decrement, skip if not zero} \\
\hline INCFSZ & PORTA, F & \multicolumn{2}{|l|}{increment, skip if zero} \\
\hline INFSNZ & PORTA, F & \multicolumn{2}{|l|}{increment, skip if not zero} \\
\hline \multicolumn{2}{|l|}{BTFSC PORTA, 5} & \multicolumn{2}{|l|}{Bit Test f, Skip if Clear} \\
\hline \multicolumn{2}{|l|}{BTFSS PORTA, 1} & \multicolumn{2}{|l|}{Bit Test f , Skip if Set} \\
\hline \multicolumn{4}{|l|}{Flow Control} \\
\hline \multicolumn{2}{|l|}{GOTO Label} & \multicolumn{2}{|l|}{Go to Address 1st word} \\
\hline \multicolumn{2}{|l|}{CALL Label} & \multicolumn{2}{|l|}{Call Subroutine 1st word} \\
\hline \multicolumn{2}{|l|}{RETURN} & \multicolumn{2}{|l|}{Return from Subroutine} \\
\hline RETLW & \(\times 23\) & \multicolumn{2}{|l|}{Return with 0x23 in WREG} \\
\hline
\end{tabular}```

