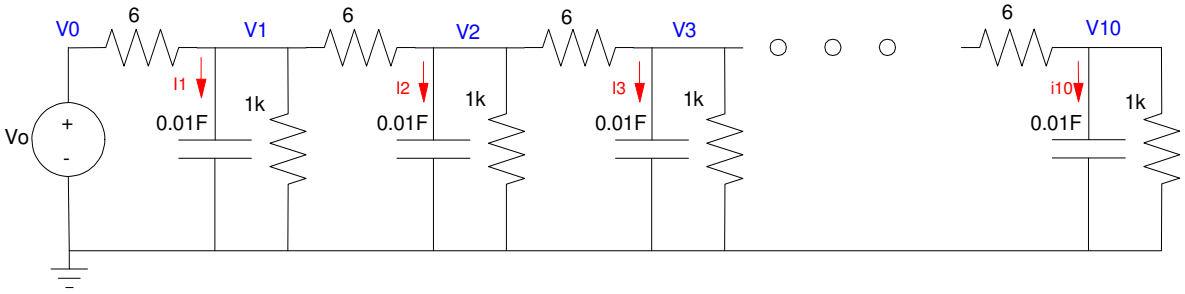
Homework #7: ECE 461/661

Gain, Lead, PID Compensation. Due Monday, October 18th

A 4th-order model for the following 10-stage RC filter is

$$G(s) = \left(\frac{170}{(s+0.47)(s+3.40)(s+9.00)(s+16.77)} \right)$$



1) Design a gain compensator (K(s) = k) which results in

- The fastest system possible,
- With no overshoot for a step input (i.e. design for the breakaway point)

For this value of k, determine

- The closed-loop dominant pole(s)
- The 2% settling time,
- The error constant, Kp, and
- The steady-state error for a step input.

Check your design in Matlab or Simulink or VisSim

2) Design a gain compensator (K(s) = k) which results in 20% overshoot for a step input. For this value of k, determine

- The closed-loop dominant pole(s)
- The 2% settling time,
- The error constant, Kp, and
- The steady-state error for a step input.

Check your design in Matlab or Simulink or VisSim

3)) Design a lead compensator, $K(s) = k\left(\frac{s+a}{s+10a}\right)$, which results in 20% overshoot for a step input. For this K(s), determine

- The closed-loop dominant pole(s)
- The 2% settling time,
- The error constant, Kp, and
- The steady-state error for a step input.

Check your design in Matlab or Simulink or VisSim

Give an op-amp circuit to implement K(s)

I Compensation

4) Design an I compensator, $K(s) = \frac{I}{s}$, which results in 20% overshoot for a step input. For this K(s), determine

- The closed-loop dominant pole(s)
- The 2% settling time,
- The error constant, Kp, and
- The steady-state error for a step input.

Check your design in Matlab or Simulink or VisSim

Give an op-amp circuit to implement K(s)

PI Compensation

5) Design a PI compensator, $K(s) = k(\frac{s+a}{s})$, which results in 20% overshoot for a step input. For this K(s), determine

- The closed-loop dominant pole(s)
- The 2% settling time,
- The error constant, Kp, and
- The steady-state error for a step input.

Check your design in Matlab or Simulink or VisSim

Give an op-amp circuit to implement K(s)