Homework #11: ECE 461/661

Digital PID Control. Due Monday, November 13th

PID Control

Assume T = 0.1 seconds:

$$G(s) = \left(\frac{9111}{(s+1.21)(s+9.02)(s+23.95)(s+44.67)} \right)$$

1) Design a digital I controller

$$K(z) = k\left(\frac{z}{z-1} \right)$$

that results in 20% overshoot in the step response.

Simulate the step response of the closed-loop system (VisSim or Simulink preferred with K(z)*G(s))

2) Assume T = 0.1 seconds and

$$G(s) = \left(\frac{9111}{(s+1.21)(s+9.02)(s+23.95)(s+44.67)} \right)$$

Design a digital PI controller

$$K(z) = k\left(\frac{z-a}{z-1} \right)$$

that results in 20% overshoot in the step response.

Simulate the step response of the closed-loop system (VisSim or Simulink preferred with K(z)*G(s))

3) Assume T = 0.1 seconds and

$$G(s) = \left(\frac{9111}{(s+1.21)(s+9.02)(s+23.95)(s+44.67)} \right)$$

Design a digital PID controller

$$K(z) = k\left(\frac{(z-a)(z-b)}{z(z-1)} \right)$$

that results in 20% overshoot in the step response.

Simulate the step response of the closed-loop system (VisSim or Simulink preferred with K(z)*G(s))

Meeting Design Specs

4) Assume a sampling rate of T = 0.1 seconds and

$$G(s) = \left(\frac{9111}{(s+1.21)(s+9.02)(s+23.95)(s+44.67)} \right)$$

Design a digital controller that results in

- No error for a step input
- 20% overshoot for the step response, and
- A 2% settling time of 2 seconds

Simulate the step response of the closed-loop system (VisSim or Simulink preferred with K(z)*G(s))

5) Assume

$$G(s) = \left(\frac{9111}{(s+1.21)(s+9.02)(s+23.95)(s+44.67)} \right)$$

Design a digital controller with T = 0.2 seconds that results in

- No error for a step input
- 20% overshoot for the step response, and
- A 2% settling time of 2 seconds

Simulate the step response of the closed-loop system (VisSim or Simulink preferred with K(z)*G(s))

Note: Changing the sampling rate is a big deal: it means a complete redesign of K(z)