ECE 320 - Homework #8

DTL, TTL Logic, MOSFETs. Due Monday, October 18th

DTL Logic

1) Determine the voltages and currents for the following DTL OR gate

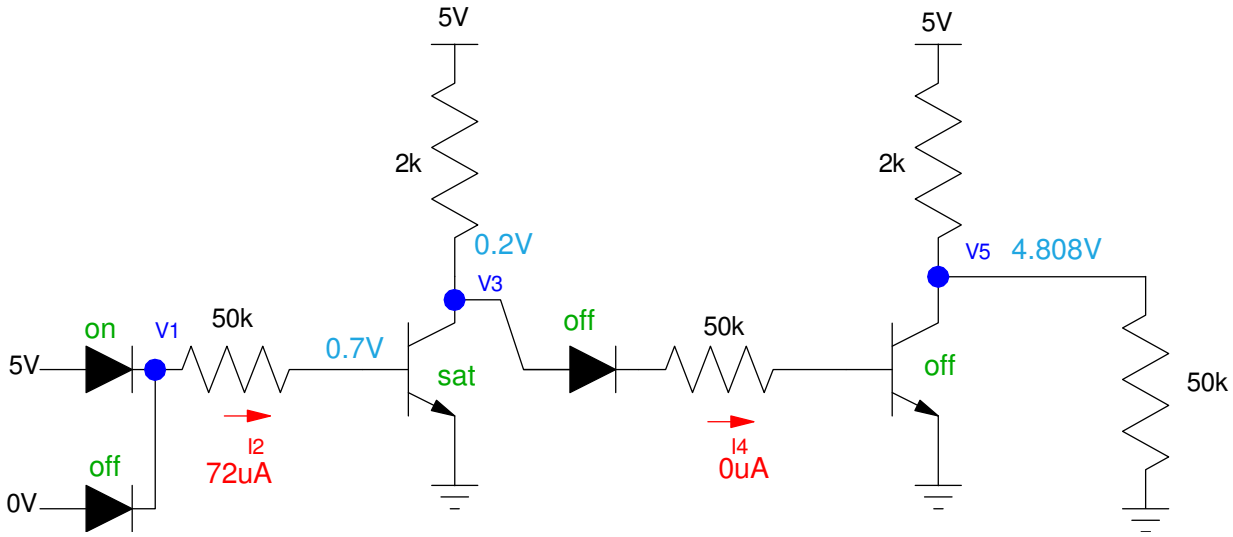
$$I_2 = \left(\frac{5V - 0.7V - 0.7V}{50k}\right) = 72uA$$

$$\beta I_2 = 14.4mA$$

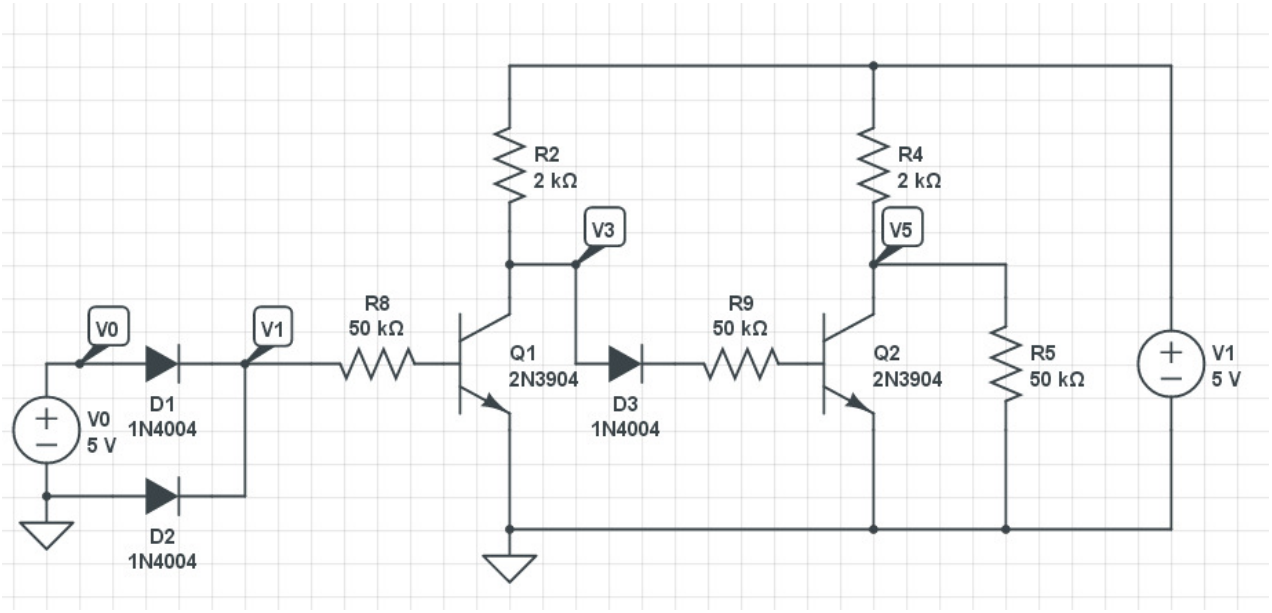
$$\max(I_c) = \left(\frac{5V - 0.2V}{2k}\right) = 2.40mA$$

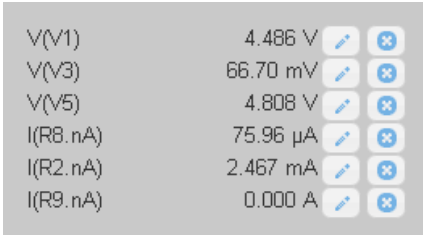
$\beta I_b > I_c$ *T1 is saturated*

$V_3 = 0.2V < 0.7V$ *T2 is off*



2) Simulate this circuit in CircuitLab to verify your answers for problem #1



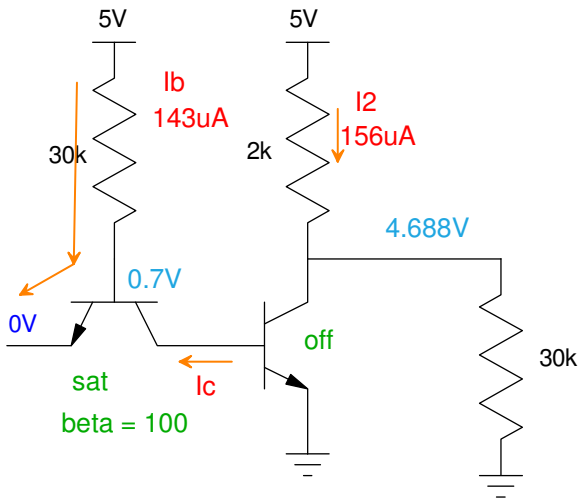


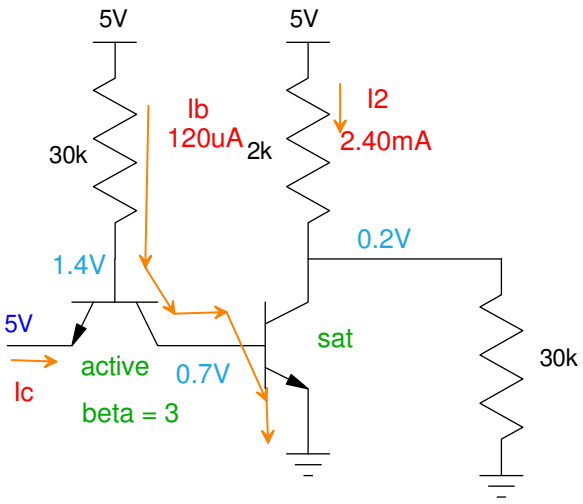
	Calculated	Simulated
V1	4.30V	4.486V
V3	0.20V	0.067V
V5	4.808V	4.808V
I(R8)	72uA	75.96uA
I(R2)	2.40mA	2.467mA
I(R9)	0	0

TTL Logic

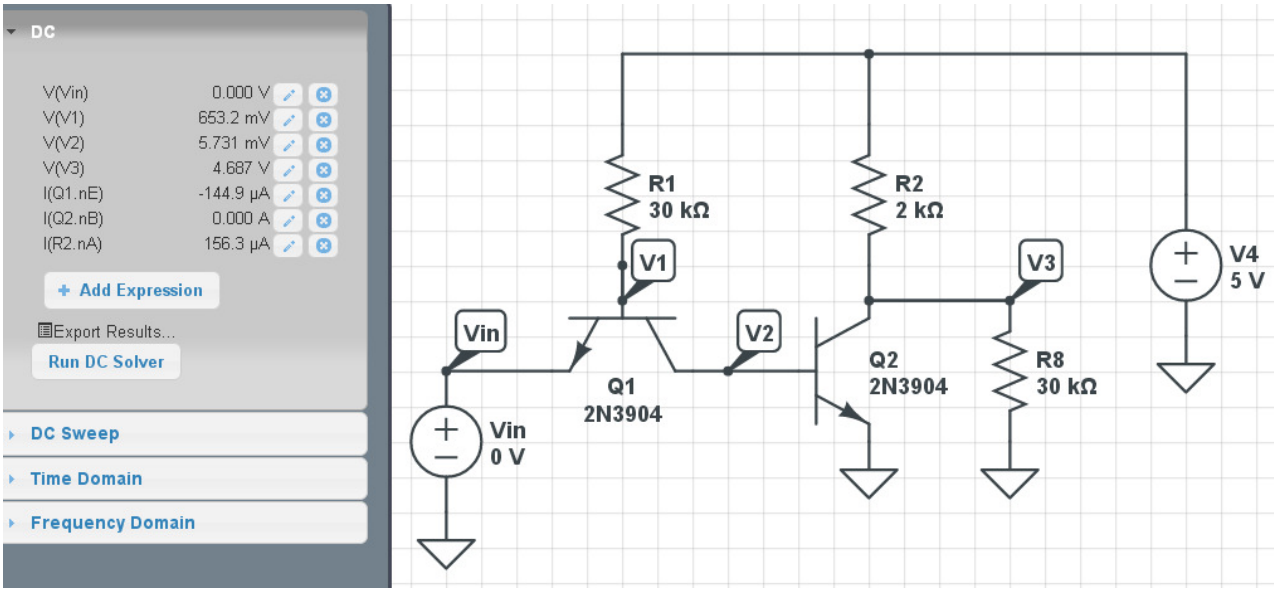
3) Determine the voltages for the following TTL inverter. Assume 3904 transistors.

Left Circuit	Right Circuit
• $I_b = \left(\frac{5V-0.7V}{30k}\right) = 143\mu A$	$I_b = \left(\frac{5V-1.4V}{30k}\right) = 120\mu A$
• $I_c = 0$	$I_c = \beta I_b = 360\mu A$
• This turns on (saturates) T1	T2 now has a base current of 480uA
• $V_c = \left(\frac{30k}{30k+2k}\right)5V = 4.688V$	which allows 48mA to flow
• $I_2 = \left(\frac{5V}{32k}\right) = 156\mu A$	max(I2) = 2.40mA (T2 is saturated)

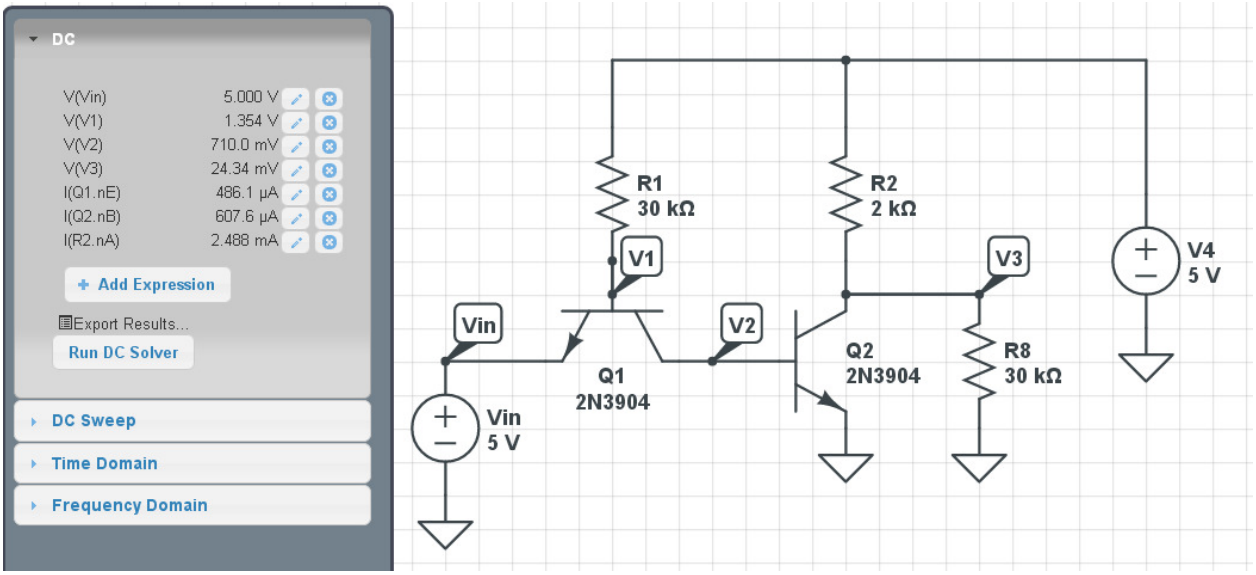




4) Simulate these circuits in CircuitLab and determine the voltage and currents



	V1	V2	V3	I(Q1.e)	I(Q2.b)	I(R2)
Calculated	0.7V	?	4.688V	143uA	0	156uA
Simulated	0.6532V	5.731V	4.687V	-144.9uA	0	156.3uA



	V1	V2	V3	I(Q1.e)	I(Q2.b)	I(R2)
Calculated	1.40V	0.70V	0.20V	360uA	480uA	2.40mA
Simulated	1.354V	0.710V	0.0234V	486uA	607uA	2.488mA

note: CircuitLab uses β=5.00 when used backwards for Q1

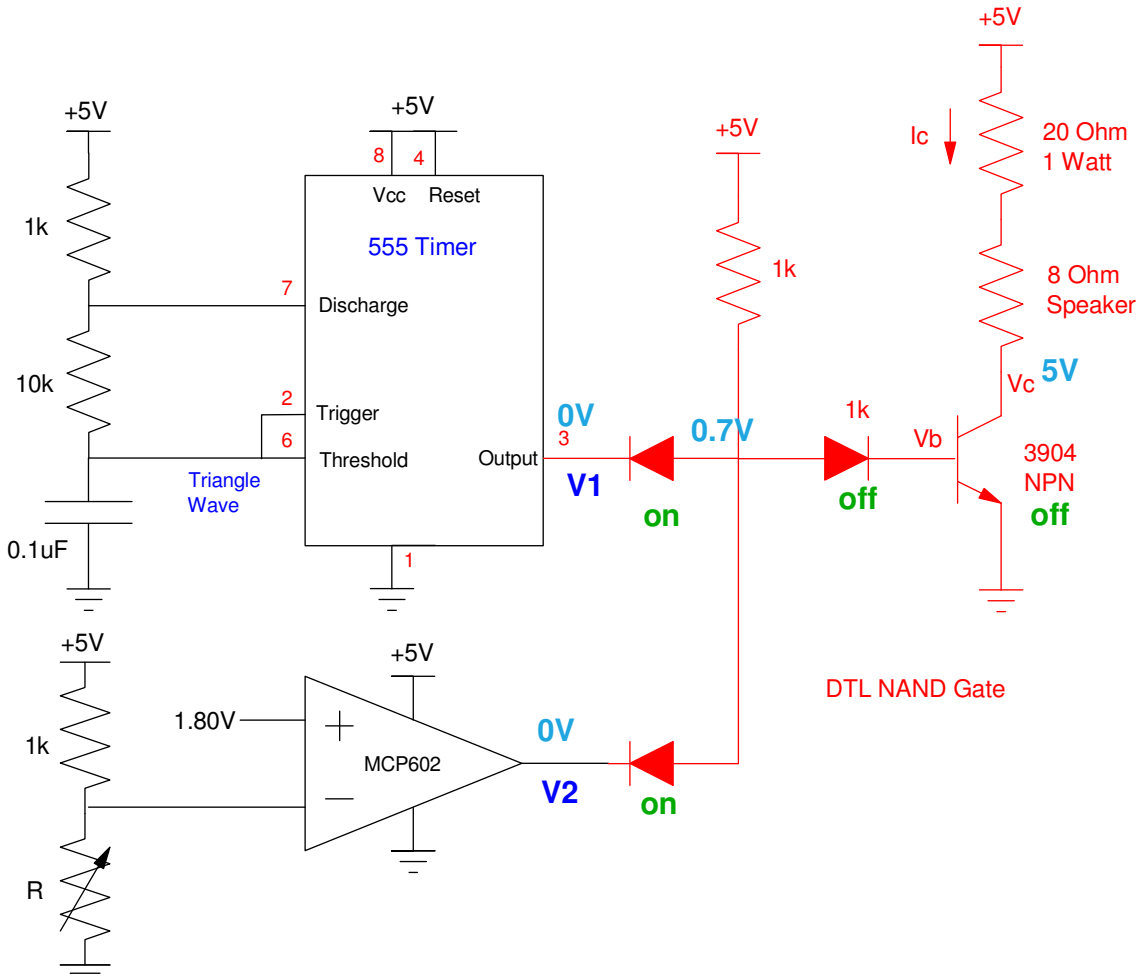
Temperature Alarm using DTL Logic

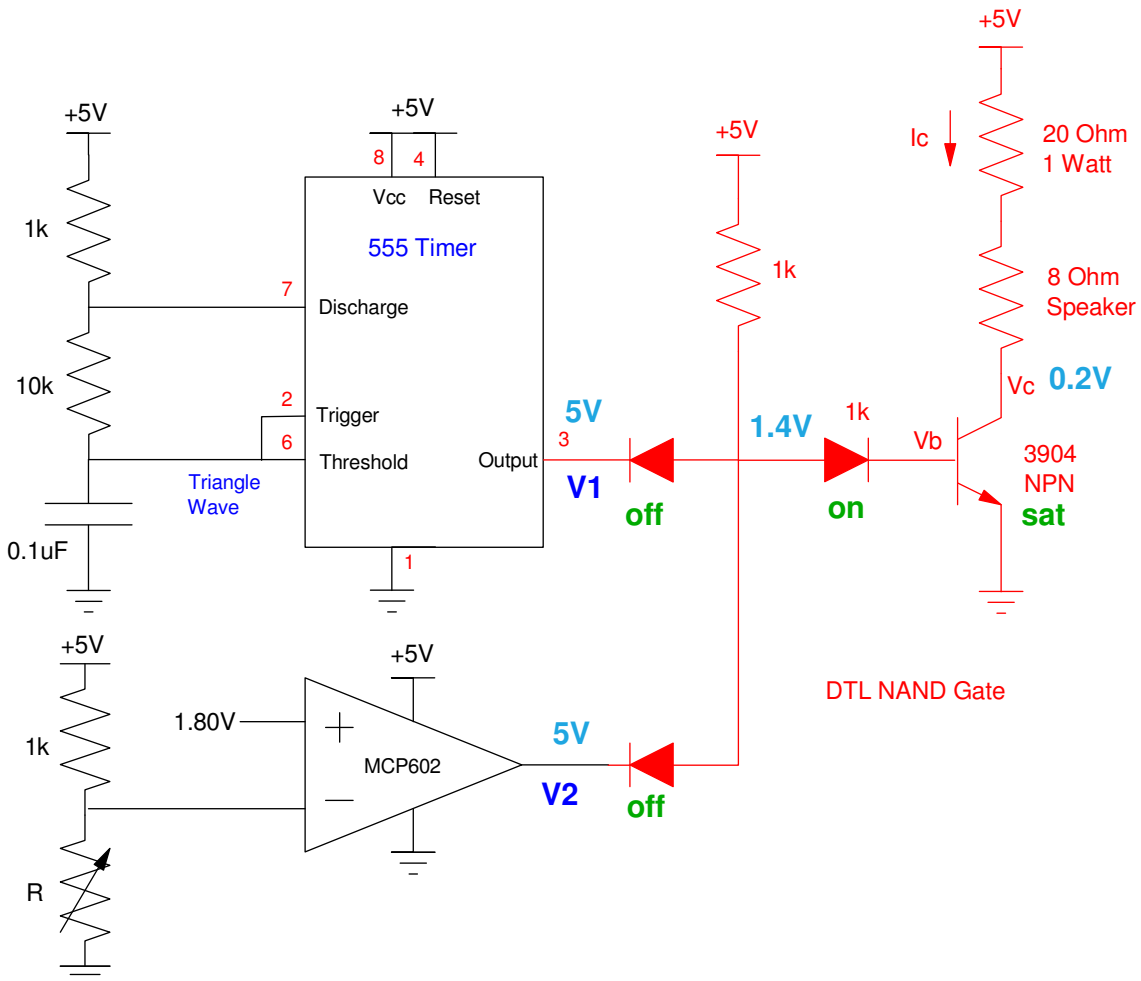
The circuit below uses a DTL NAND gate to drive the speaker when

- The 555 timer outputs 5V, and
- The comparitor outputs 5V,.

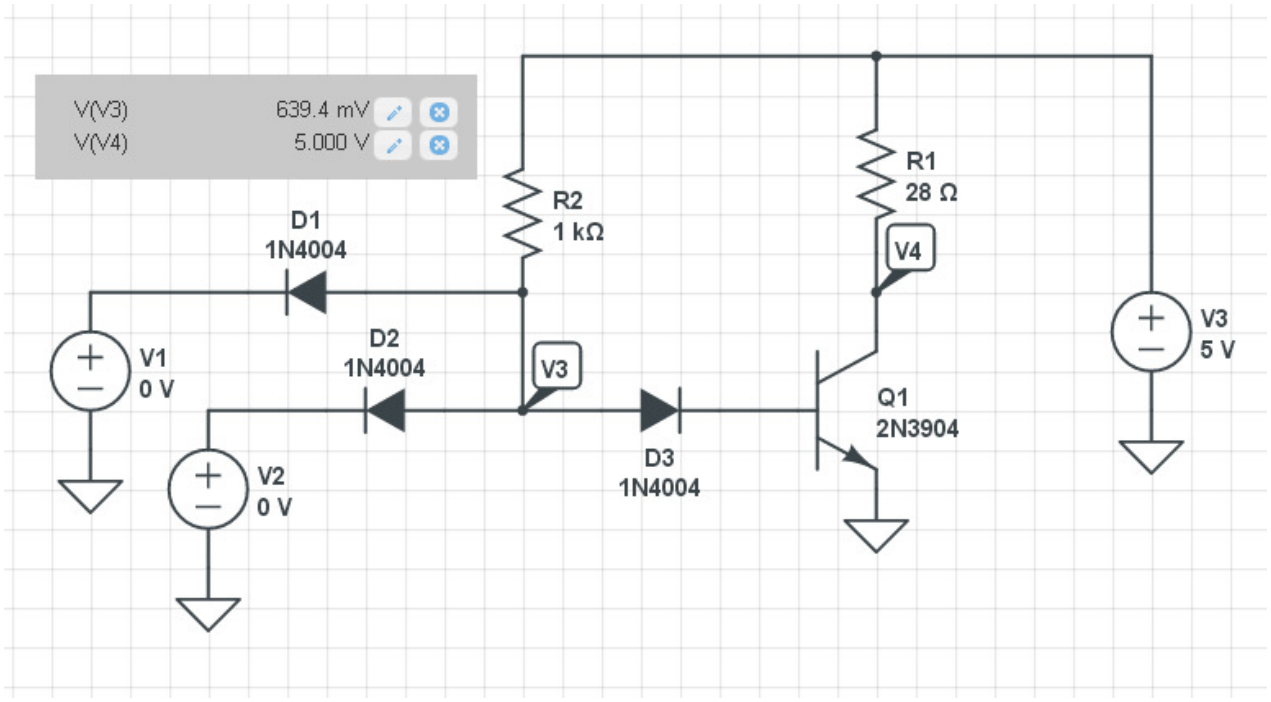
5) Determine the voltages when

- V1 = V2 = 0V
- V1 = V2 = 5V
- V1 = 0V, V2 = 5V




+5V
1k
10k
0.1uF
Triangle
Wave
+5V
8
4
Vcc
Reset
555 Timer
7
Discharge
2
Trigger
6
Threshold
Output
3
1
5V
V1
off
+5V
1k
1.4V
1k
on
Vb
+5V
Ic
20 Ohm
1 Watt
8 Ohm
Speaker
Vc
0.2V
3904
NPN
sat
DTL NAND Gate
+5V
1k
R
1.80V
MCP602
+5V
5V
V2
off

6) Verify your design using CircutiLab.



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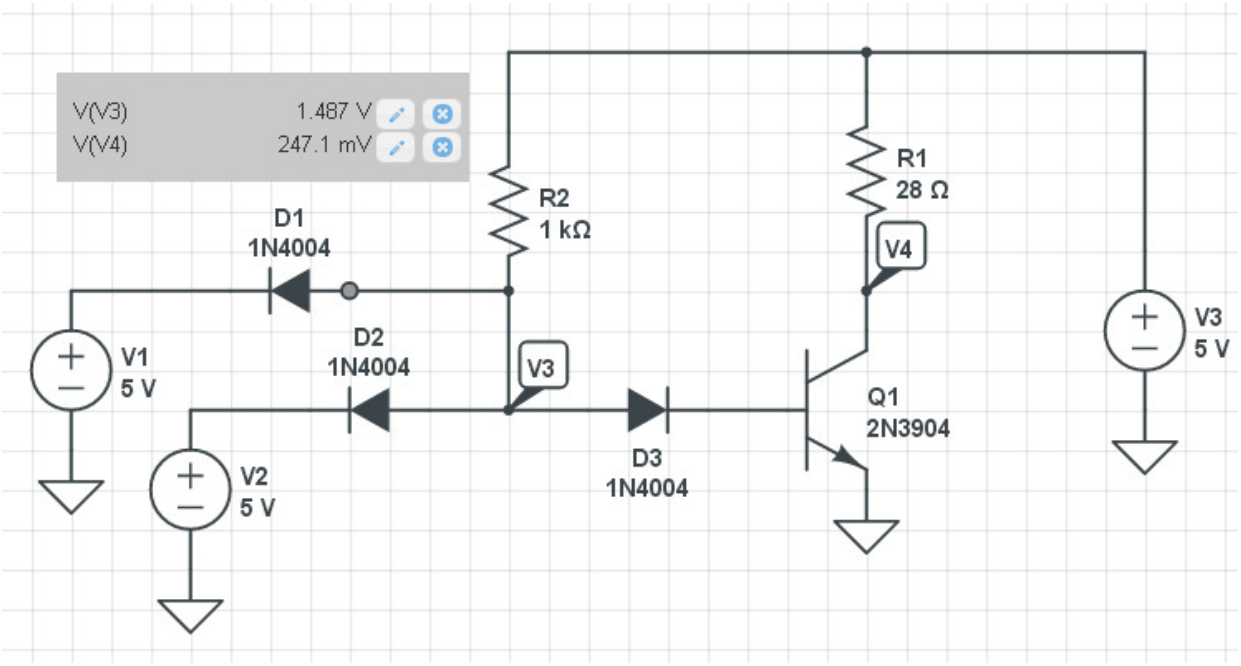
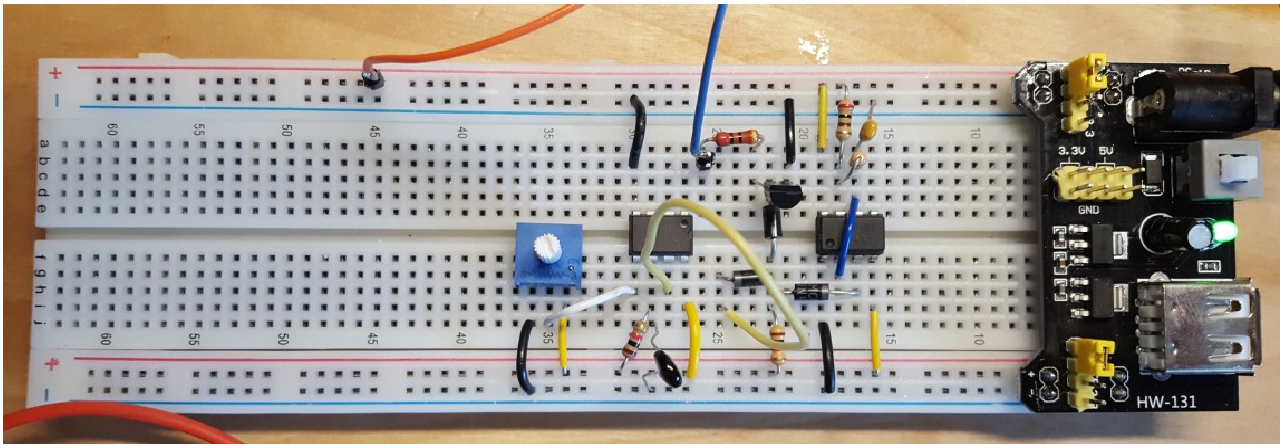
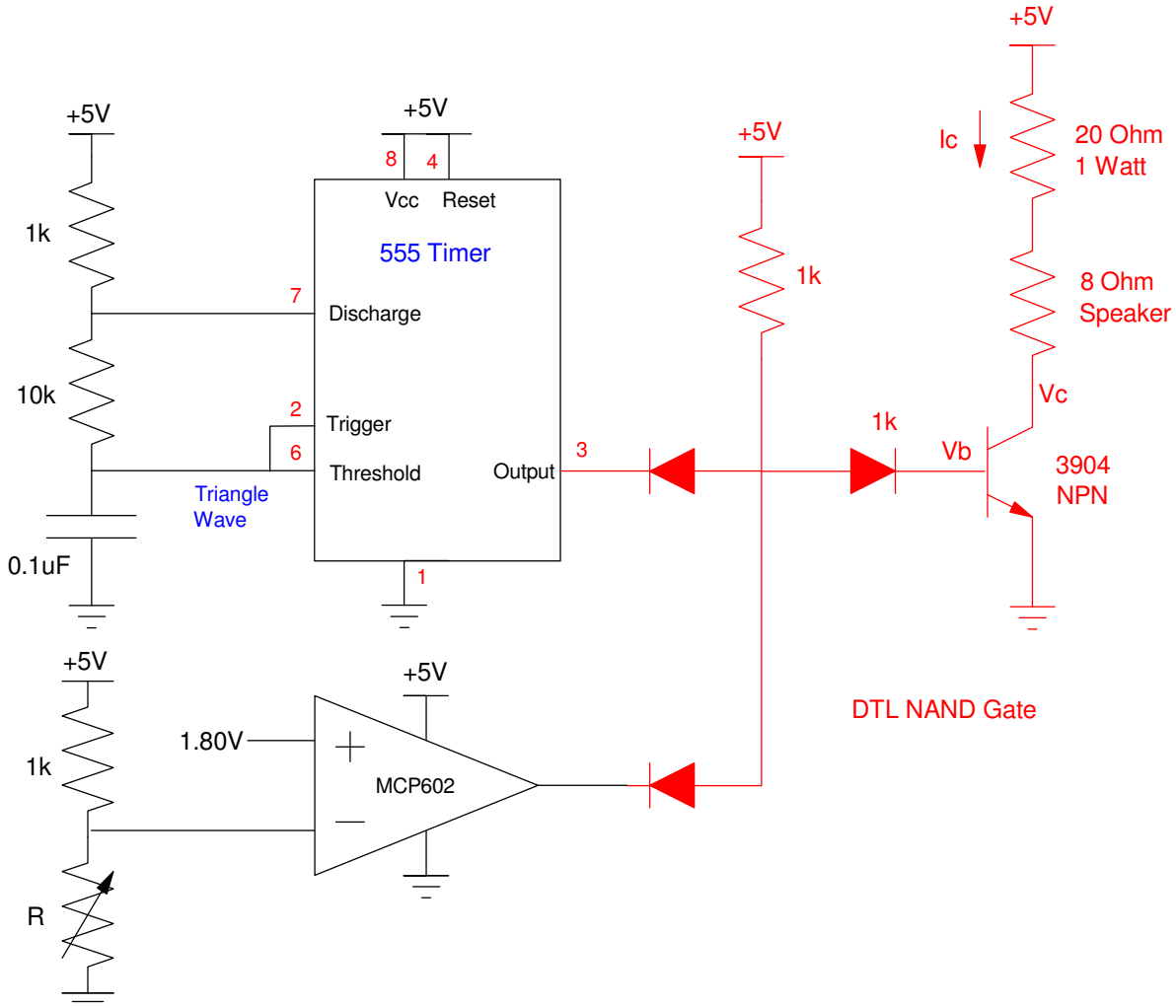


Lab: 7) (20pt): Verify your design in hardware (build and test the circuit with your lab kit).





- The 555 timer from homework set #5 for V1, and
- Connecting theThe comparitor from homework set #5 for V2

Verify that

- The speaker turns on when T > Ton and
- The speaker turns off when T < Ton

Setting the comparitor to turn on at 1.80V

- Speaker turns on when Vr < 1.80V
- Speaker turns off when Vr > 1.83V
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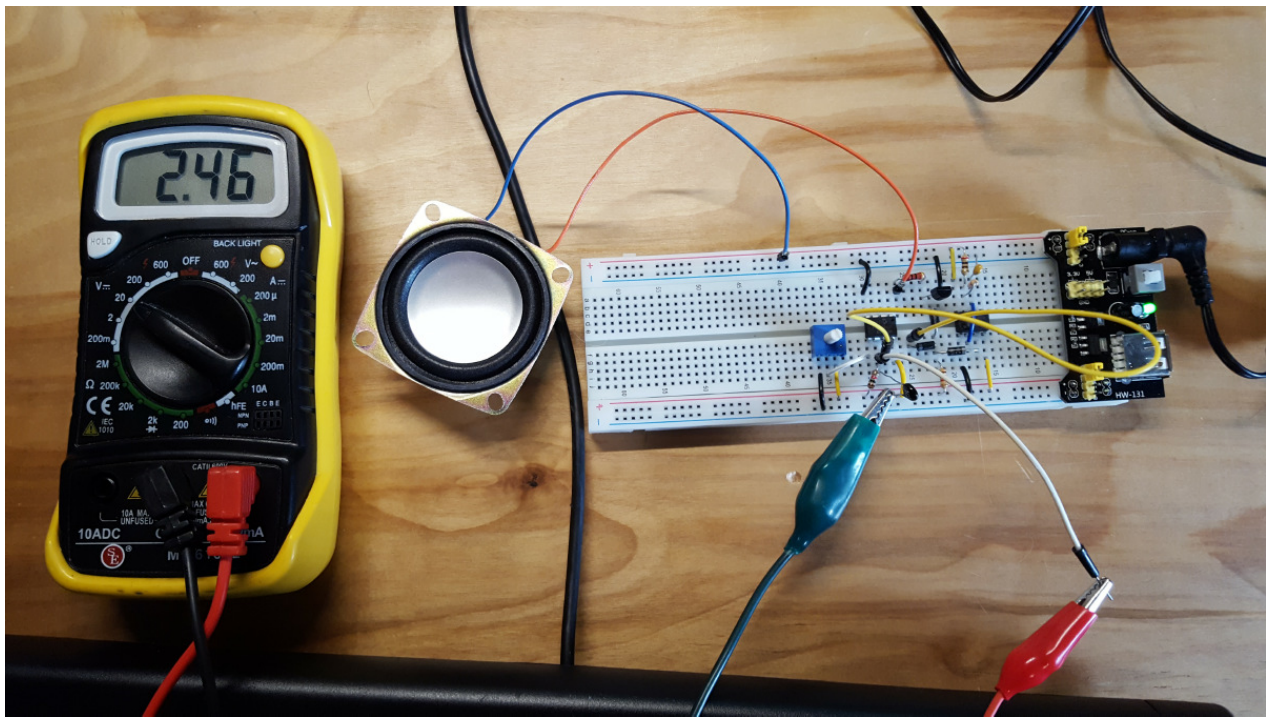


MOSFET

8) Label the operating regions on the graph below (off, ohmic, saturated) and determine the transconductance gain, kn. Assume the turn-on voltage is Vt = 1.00V

To find kn, pick a point. point A (Ohmic region)

$$I_{ds} = k_n\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds}$$

$$600mA = k_n\left(7V - 1V - \frac{2V}{2}\right)2V$$

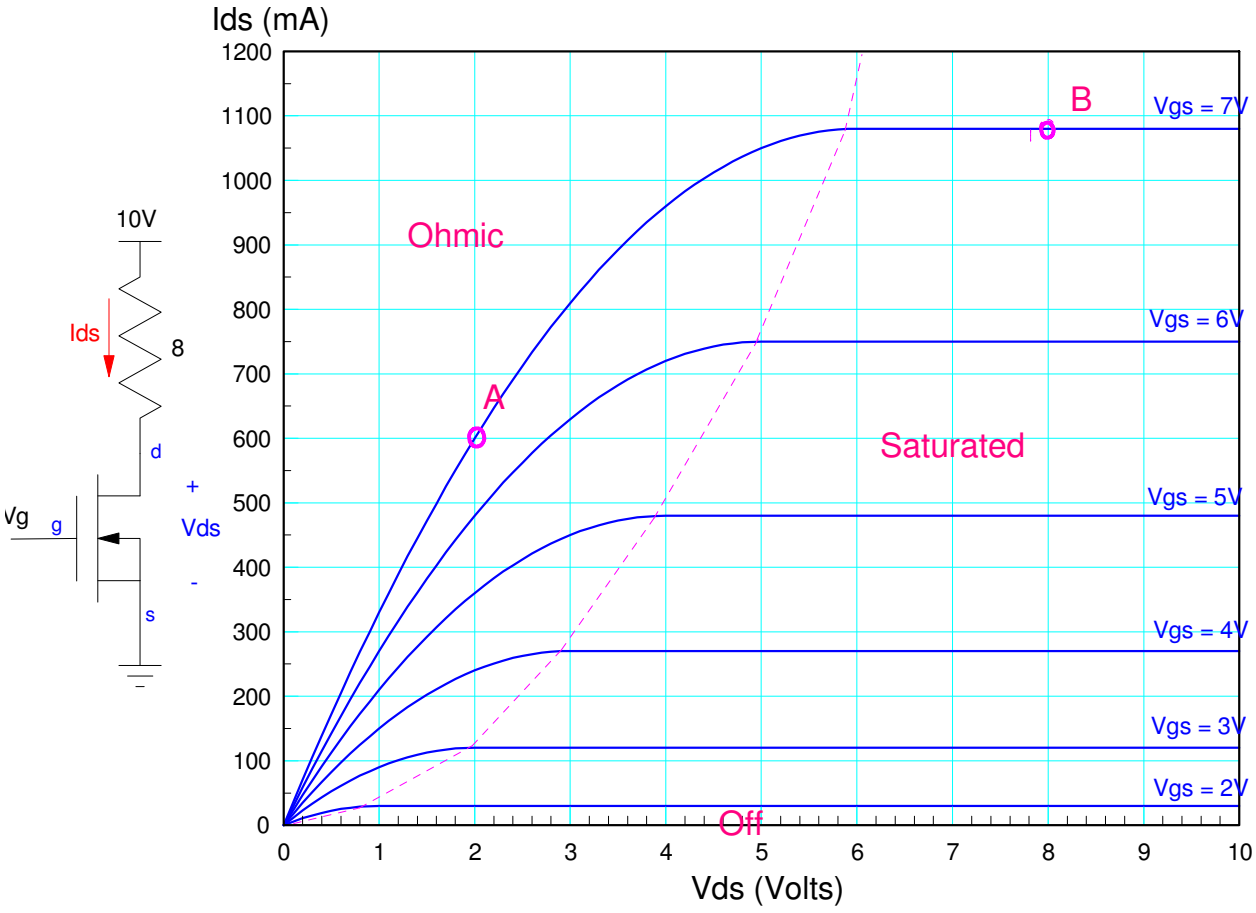
$$k_n = 0.060\frac{A}{V^2}$$

Point B (Saturated revion)

$$I_{ds} = \frac{k_n}{2}(V_{gs} - V_{th})^2$$

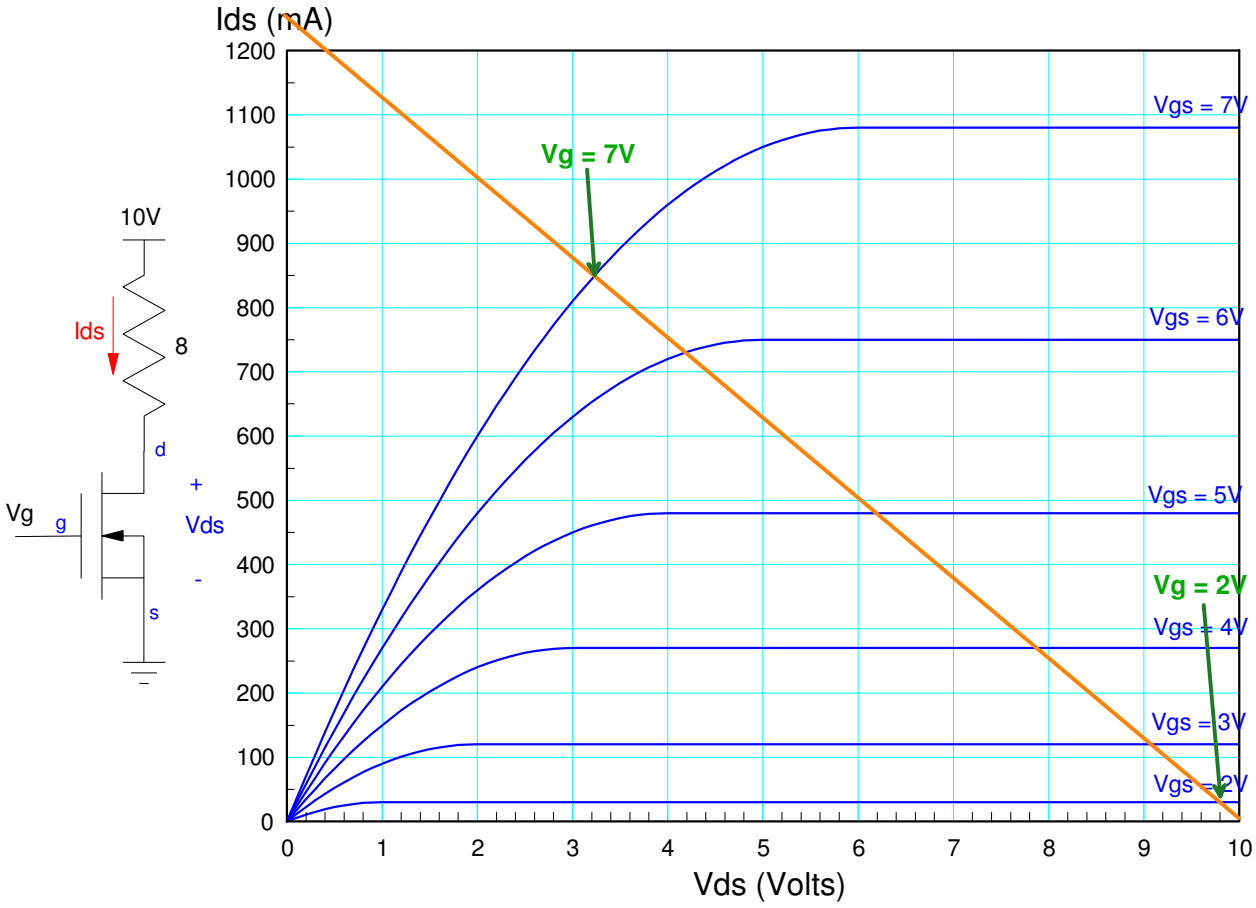
$$1080mA = \frac{k_n}{2}(7V - 1V)^2$$

$$k_n = 0.060\frac{A}{V^2}$$



9) Draw the load line for the circuit below. From the load line, determine the operating point (Vds, Ids) when

- Vg = 2V
- Vg = 7V



10) Calculate the operating point (Vds, Ids) when

Vg = 2V (Saturated region)

$$I_{ds} = \frac{k_n}{2}(V_{gs} - V_{th})^2$$

$$I_{ds} = \frac{0.06}{2}(2V - 1V)^2 = 30mA$$

$$V_{ds} = 10 - 8 \cdot I_{ds} = 9.76V$$

Vg = 7V (Ohmic region)

$$I_{ds} = k_n\left(V_{gs} - V_{th} - \frac{V_{ds}}{2}\right)V_{ds}$$

$$I_{ds} = 0.06\left(7 - 1 - \frac{V_{ds}}{2}\right)V_{ds}$$

$$V_{ds} = 10 - 8 \cdot I_{ds}$$

solving 2 equations for 2 unknowns

Vds = 3.218V

or

Vds = 12.949V

The former is the correct solution

ans

Vds = 3.218V

Ids = 848mA