

ECE 320 - Quiz #8 - Name _____

Boolean Logic, DTL, TTL Logic.

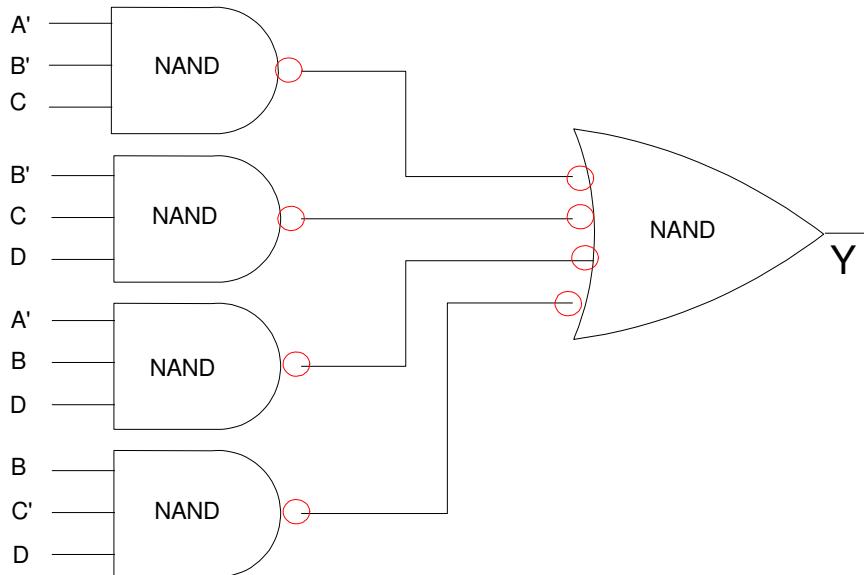
Boolean Logic

- 1) Implement the following logic using NAND gates (circuit the ones).

- $Y = 1$ if $ABCD$ is prime: $\{2, 3, 5, 7, 11, 13\}$

		CD		Y
		00	01	
AB	00	0	0	1
	01	0	1	1
11	0	1	0	0
10	0	0	1	0

$$Y = A'B'C + B'CD + A'BD + BC'D$$



Boolean Logic

2) Implement the following logic using NOR gates (circuit the zeros).

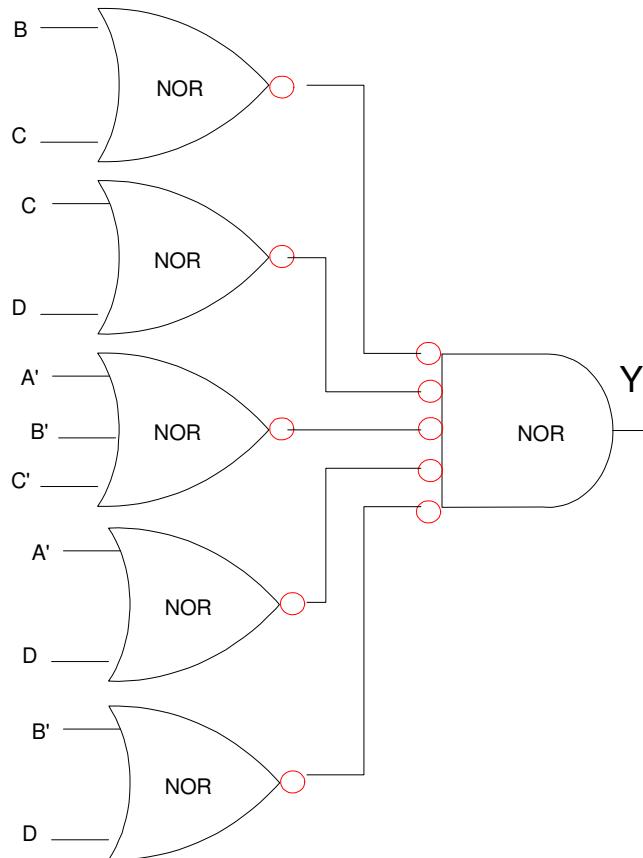
- $Y = 1$ if $ABCD$ is prime: $\{2, 3, 5, 7, 11, 13\}$

		CD		Y		
		00	01	11	10	
AB		00	0	0	1	1
01	01	0	0	1	1	0
11	11	0	0	1	0	0
0	0	0	0	1	0	0

$$Y' = B'C' + C'D' + ABC + AD' + BD'$$

using DeMorgan's theorem

$$Y = (B + C)(C + D)(A' + B' + C')(A' + D)(B' + D)$$

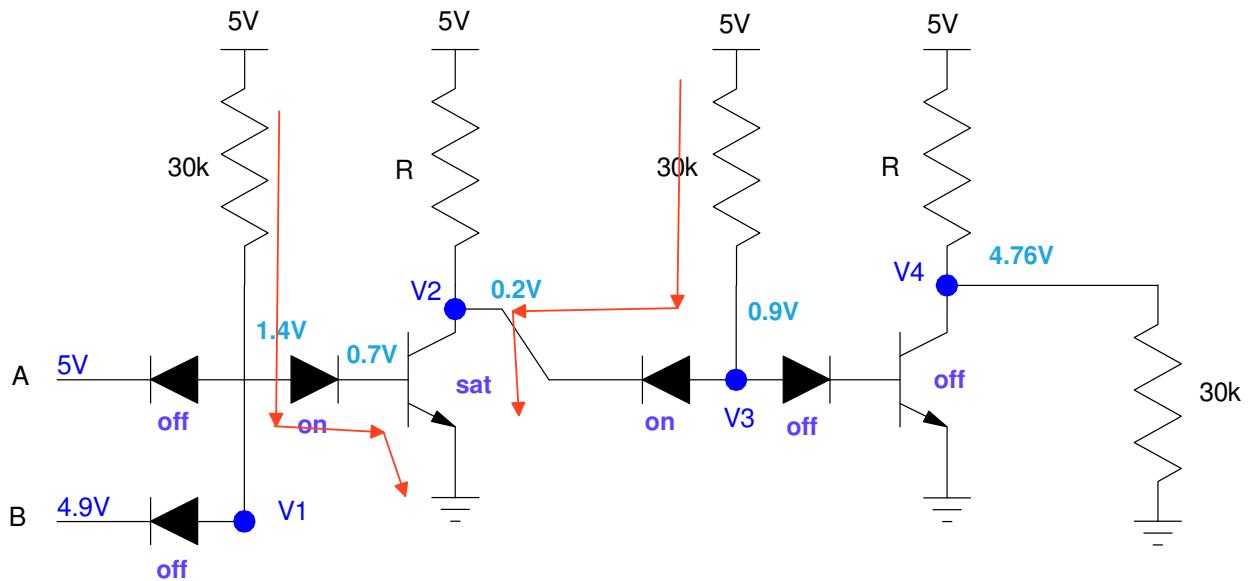


DTL Logic Gate:

3) Determine the voltages and currents for the following DTL gate. Assume

- Ideal 3904 transistors ($V_{be} = 0.7V$, $V_{ce(sat)} = 0.2V$, gain = 100)
- Ideal silicon diodes ($V_f = 0.7V$)
- $R = 1000 + 100(\text{Birth Month}) + (\text{Birth Day})$. For example, May 14th gives $R = 1514$ Ohms.

R	V1	V2	V3	V4
1514	1.4V	0.2V T1 saturated	0.9V	4.76V T2 off

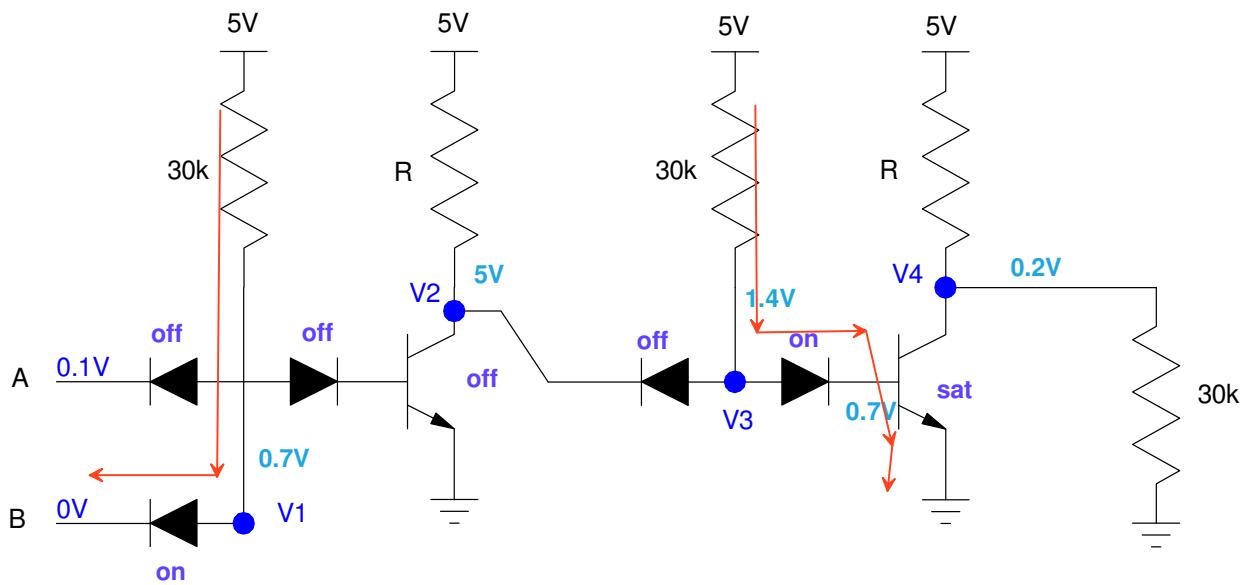


DTL Logic Gate:

4) Determine the voltages and currents for the following DTL gate. Assume

- Ideal 3904 transistors ($V_{be} = 0.7V$, $V_{ce(sat)} = 0.2V$, gain = 100)
- Ideal silicon diodes ($V_f = 0.7V$)
- $R = 1000 + 100(\text{Birth Month}) + (\text{Birth Day})$. For example, May 14th gives $R = 1514$ Ohms.

R	V1	V2	V3	V4
1514	0.7V	5V	1.4V	0.2V

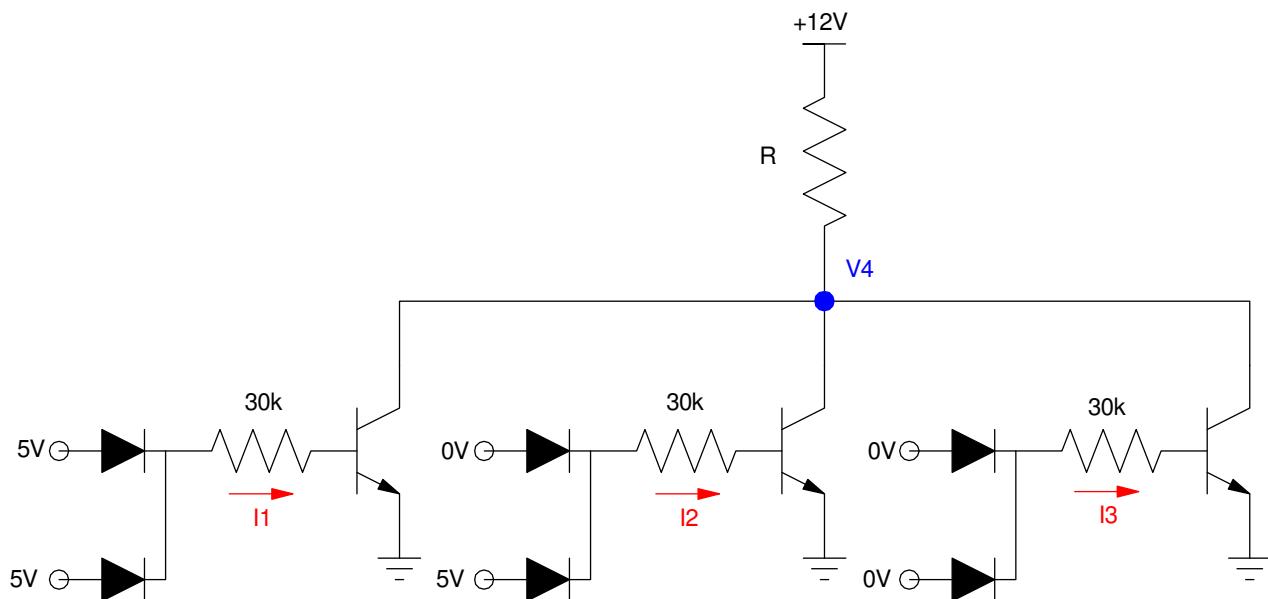


Open Collector Logic

5) Determine the voltages and currents for the following circuit. Assume

- Ideal silicon diodes ($V_f = 0.7V$)
- $V_{be} = 0.7V$
- $\beta = 100$
- $R = 1000 + 100(\text{Birth Month}) + (\text{Birth Day})$. For example, May 14th gives $R = 1514$ Ohms.

R	I1	I2	I3	V4
1514	120uA	120uA	0	0.2V saturated



$$I_1 = \left(\frac{5V - 1.4V}{30k} \right) = 120\mu A$$

$$I_2 = \left(\frac{5V - 1.4V}{30k} \right) = 120\mu A$$

$$I_3 = 0$$

$$I_R = \left(\frac{12V - 0.2V}{1514} \right) = 7.794mA$$

Check that the transistors are saturated

$$\beta I_b = 100 \cdot 120\mu A = 12mA \quad (\text{x 2 meaning the transistors together allow } 24mA \text{ to flow})$$

$$24mA > 7.74mA \quad \text{saturated}$$

TTL Logic

6) Determine the voltages and currents for the following DTL gate. Assume

- Ideal 3904 transistors ($V_{be} = 0.7V$, $V_{ce(sat)} = 0.2V$, $\beta = 2$ (left) or 100 (right) transistor
- $R = 1000 + 100(\text{Birth Month}) + (\text{Birth Day})$. For example, May 14th gives $R = 1514$ Ohms.

R	V1	V2	V3	V4
1514	4.273V	1.4V	0.7V	0.2V

