

# ECE 320 - Quiz #8 - Name \_\_\_\_\_

Boolean Logic, DTL, TTL Logic, MOSFETs.

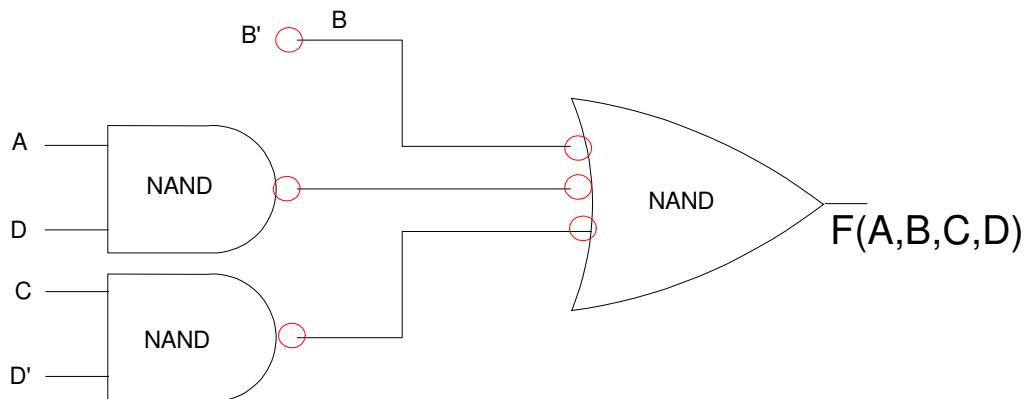
## Boolean Logic

- 1) Design a circuit using NAND gates to implement the following logic

$f(A,B,C,D)$

|    |    | CD |    |    |    |
|----|----|----|----|----|----|
|    |    | 00 | 01 | 11 | 10 |
| AB | 00 | x  | x  | x  | 1  |
|    | 01 | 0  | 0  | 0  | x  |
|    | 11 | 0  | 1  | 1  | 1  |
|    | 10 | 1  | x  | x  | x  |

$$f = \overline{B} + AD + CD$$



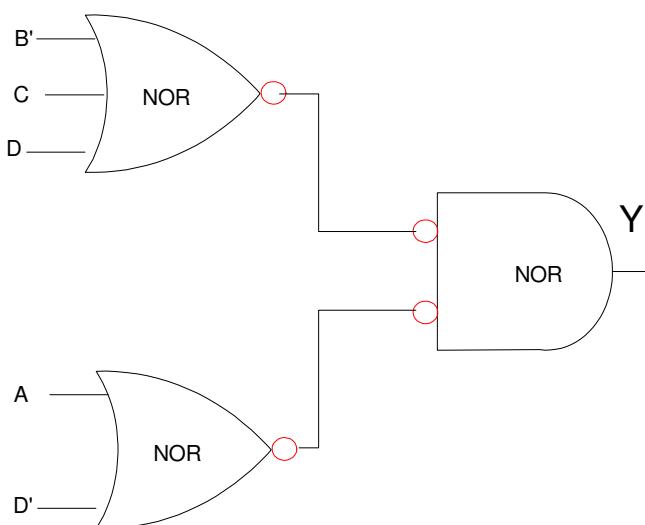
2) Design a circuit using NOR gates to implement the following logic:

$Y(A,B,C,D)$

|    |  | 00 | 01 | 11 | 10 | CD |
|----|--|----|----|----|----|----|
|    |  | AB | 00 | 01 | 11 | 10 |
|    |  | 00 | x  | x  | x  | 1  |
| AB |  | 01 | 0  | 0  | 0  | x  |
|    |  | 11 | 0  | 1  | 1  | 1  |
|    |  | 10 | 1  | x  | x  | x  |

$$\bar{Y} = B\bar{C}\bar{D} + \bar{A}D$$

$$Y = (\bar{B} + C + D)(A + \bar{D})$$

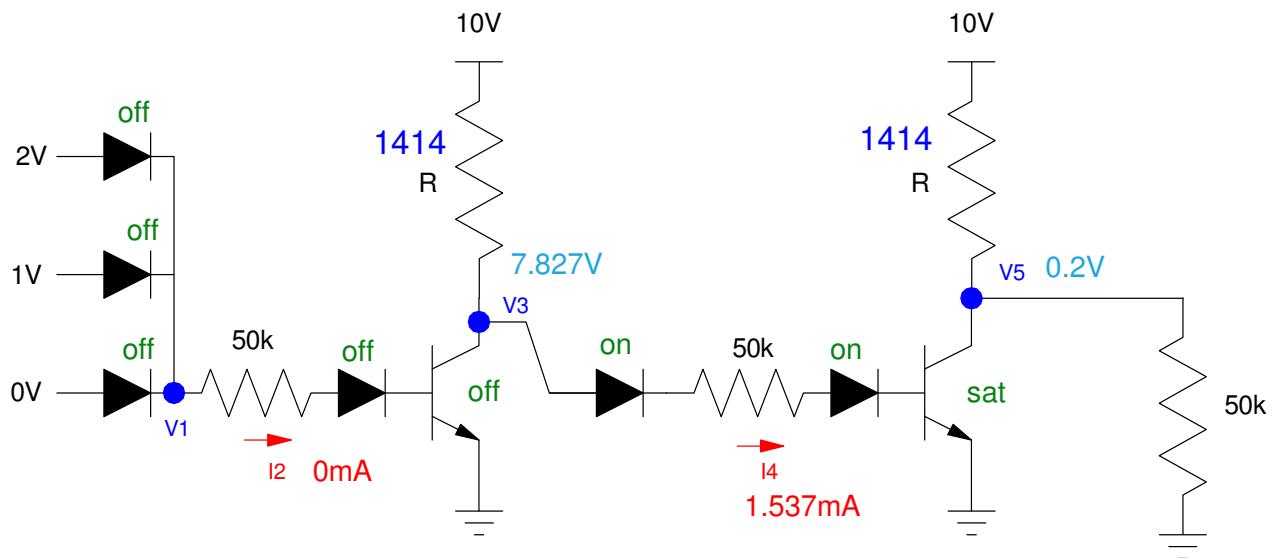


## DTL: 10V Logic Logic

3) Determine the voltges and currents for the following DTL gate. Assume

- Ideal 3904 transistors ( $V_{be} = 0.7V$ ,  $V_{ce(sat)} = 0.2V$ , gain = 100)
- Ideal silicon diodes ( $V_f = 0.7V$ )
- $R = 900 + 100(\text{Birth Month}) + (\text{Birth Day})$ .

| $R$<br>$900 + 100 \cdot \text{mo} + \text{day}$ | $V_1$                        | $I_2$    | $V_3$         | $I_4$          | $V_5$       |
|---|------------------------------|----------|---------------|----------------|-------------|
| <b>1414</b>                                     | <b>1.3..1.4V</b><br>floating | <b>0</b> | <b>7.827V</b> | <b>1.537mA</b> | <b>0.2V</b> |



$$I_4 = \left( \frac{10V - 2.1V}{50k + 1414} \right) = 1.537mA$$

$$V_3 = 10V - 1414 \cdot 1.537mA$$

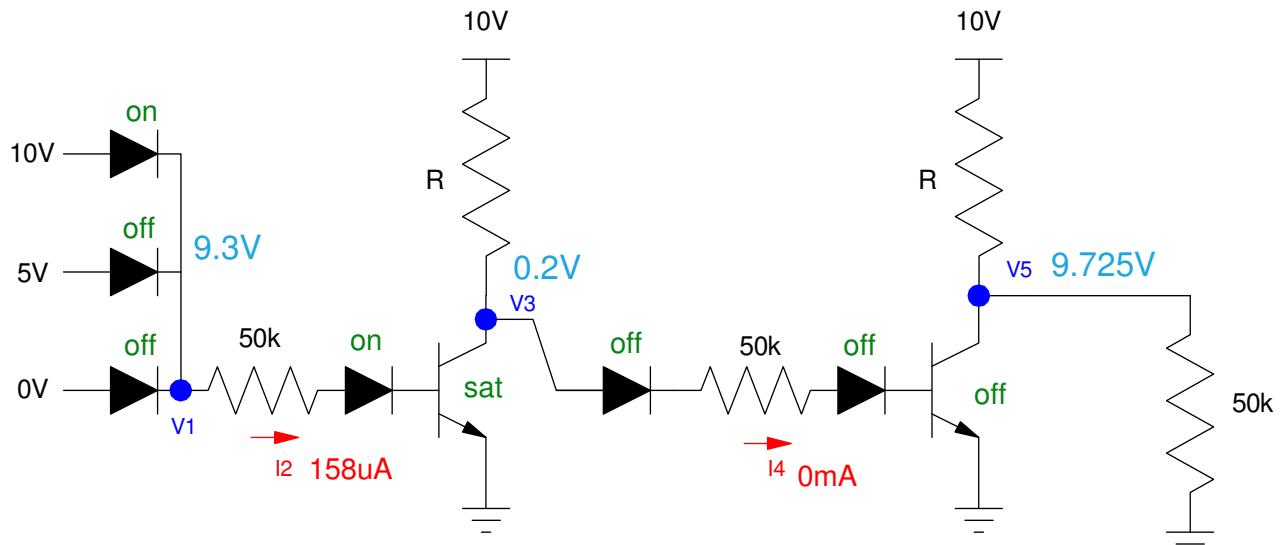
$$V_3 = 7.827V$$

## DTL 10V Logic Gate:

4) Determine the voltages and currents for the following DTL gate. Assume

- Ideal 3904 transistors ( $V_{be} = 0.7V$ ,  $V_{ce(sat)} = 0.2V$ , gain = 100)
- Ideal silicon diodes ( $V_f = 0.7V$ )
- $R = 900 + 100(\text{Birth Month}) + (\text{Birth Day})$ .

| $R$<br>$900 + 100 \cdot \text{mo} + \text{day}$ | $V_1$        | $I_2$        | $V_3$       | $I_4$    | $V_5$         |
|---|--------------|--------------|-------------|----------|---------------|
| <b>1414</b>                                     | <b>9.30V</b> | <b>158uA</b> | <b>0.2V</b> | <b>0</b> | <b>9.725V</b> |



$$I_2 = \left( \frac{10V - 2.1V}{50k} \right) = 158\mu A$$

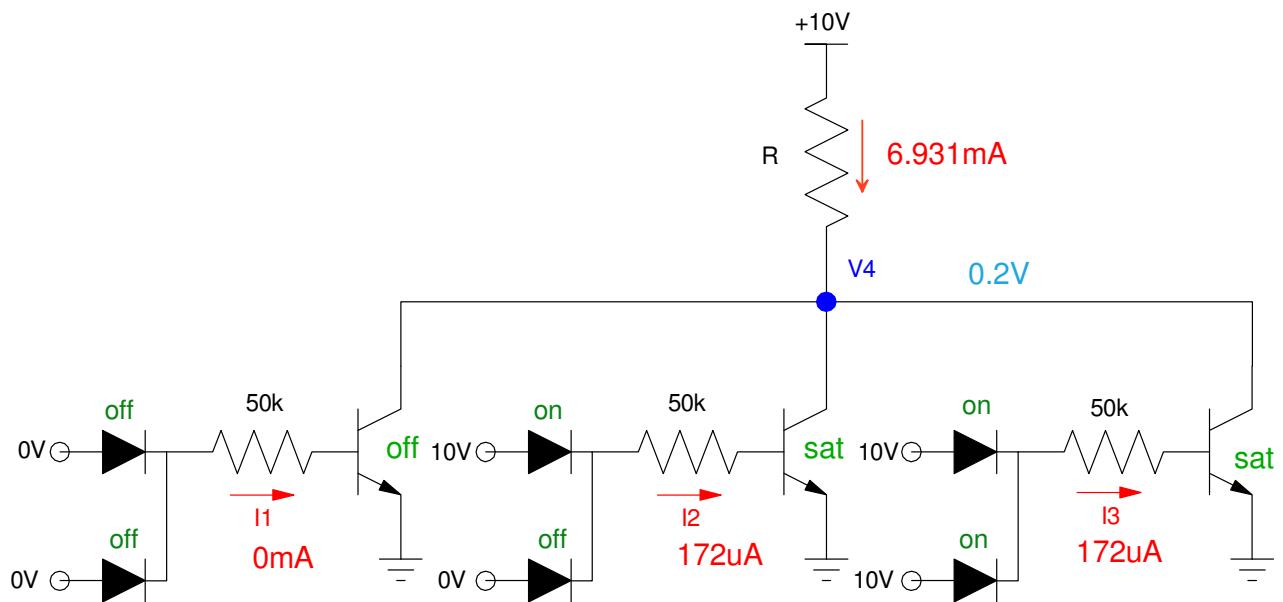
$$V_5 = \left( \frac{50k}{50k + 1414} \right) 10V = 9.725V$$

## 10V Open Collector Logic

5) Determine the voltages and currents for the following circuit. Assume

- Ideal silicon diodes ( $V_f = 0.7V$ )
- $V_{be} = 0.7V$
- $\beta = 100$
- $R = 900 + 100(\text{Birth Month}) + (\text{Birth Day})$ .

| $R$<br>$900 + 100 \cdot \text{mo} + \text{day}$ | $I_1$    | $I_2$        | $I_3$        | $V_4$       |
|---|----------|--------------|--------------|-------------|
| <b>1414</b>                                     | <b>0</b> | <b>172uA</b> | <b>172uA</b> | <b>0.2V</b> |



## TTL Logic

6) Determine the voltages and currents for the following TTL gate. Assume

- Ideal 3904 transistors ( $V_{be} = 0.7V$ ,  $V_{ce(sat)} = 0.2V$ ,  $\beta = 100$ )
- $R = 900 + 100(\text{Birth Month}) + (\text{Birth Day})$ .

| $R$<br>$900 + 100 \cdot \text{mo} + \text{day}$ | $V_1$       | $V_2$                         | $V_3$         | $I_4$      |
|---|-------------|-------------------------------|---------------|------------|
| <b>1414</b>                                     | <b>0.7V</b> | <b>0V .. 0.7V</b><br>floating | <b>9.861V</b> | <b>0mA</b> |

